Sequential Switching Shunt Regulators for LEO Satellite Applications

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Abstract

This paper presents the topology and design of sequential shunt regulators for Low Earth Orbit (LEO) satellite applications. The objectives of the study are to provide main bus regulation in low-power LEO satellites and to reduce the effect of parasitic capacitance, which has become an important problem in GaAs-based multi-junction solar panels. This issue gets even more severe and widespread with the increase in satellite power needs. The bus regulation is achieved by a regulator based on the S3R topology designed in a modular way providing high reliability for space projects. It consists of five regulating stages with a power of 200 W each. In addition, a properly sized passive current limiter is added to eliminate parasitic capacitance effects. The whole design is verified via simulation. The performance under varying loads haven been truly investigated, and compliance to design inputs is compared. In conclusion, the results have demonstrated that the design of S3R regulator successfully maintains the main bus voltage under varying load conditions while providing maximum reality for space applications.

1. Introduction

In satellite systems, the electrical power system (EPS) consists of an energy source (solar panels) and an energy converter that converts this source into electricity. The sun is used as the energy source, and the power electronics-based subsystem is used as the energy converter. In addition, there are additional components that vary depending on the application. When the satellite cannot receive the sun's rays, during solar eclipses, when the solar panel arrays are not capable of providing sufficient power, or when the loads are overloaded, the rechargeable battery is used as an alternative energy source for full-capacity operation. The battery group is charged through the battery charge regulator (BCR). The charging module is not allowed to operate while the battery is discharging. During a solar eclipse, the battery is discharged to meet the satellite's power needs. The number of battery discharge modules is determined according to the peak power of the bus and the redundancy approach.

In space applications, the amount of power to be produced and the management and distribution of this power play an essential role in EPS design. In the satellite power system, electrical power must be produced sufficiently and with high power quality to power the payloads throughout the satellite's mission life. During the operation of the satellite's electrical power system, it should not affect the operation and power quality of other loads and subsystems. At the same time, it should not be affected. In an EPS design, the worst-case consumption of subsystems and payloads is taken into account when determining the power requirement of the system. At this point, two basic methods emerge: DET (Direct Energy Transfer) and MPPT (Maximum Power Point Tracking).

DET (Direct Energy Transfer method) is based on shunt regulators that keep the main bus voltage below a preset maximum value, regardless of the change in load or the difference in the solar panel. S3R is called a sequential switching shunt regulator and is used in the direct energy transfer (DET) method. S3R topology has multiple sections that work sequentially and are connected in parallel. The sections work sequentially. All but one of the cells operate in either transmit or shunt mode. Operation in switching mode occurs in only one of the sections, depending on the needs of the loads. The reason why this method is a direct energy transfer is that the solar panels are directly connected to the load bus. Since the variety and number of materials used are low, it is a relatively simple and highly reliable system. After the energy needed by the load is directed and distributed, the excess power produced is discarded.

MPPT (Maximum Power Point Tracking method) is based on the use of switched DC/DC converter photovoltaic systems controlled by the MPPT algorithm by placing a serial regulator between the solar panels and the battery. This technique adjusts the current and voltage values required to draw maximum power from the solar panels. In this method, excess energy is not wasted and remains in the panels because, in this technique, the maximum peak point is moved away as the power requirement decreases. A PWM controller is used since a serial PWM controlled regulator is used in the MPPT technique. These controllers can cause transients and noise during switching. Therefore, filters are required to suppress EMI-related noise. This adds size and weight to satellite equipment [1].

2. S3R Circuit Structure and Simulation Studies

In the simulation studies, five regulation sections were used, and the design was made for an S3R cell with a total power of 200W. Control of each regulation section is provided by the mean error amplifier (MEA), which is achieved using majority voting. Each S3R cell is activated sequentially. For example, when the main bus does not need the current from the solar panel, the relevant solar panel section is shunted with the help of the switch

controlled by MEA. The block diagram of the system is given in Fig. 1.

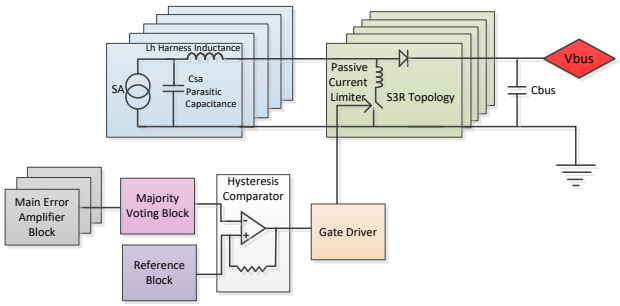

Fig. 1. Block diagram of the system

Thermal and electrical responses of the system should be considered when designing, and analysis should be included when sizing. The resonance between the inductance of the harness and the parasitic capacitance of the solar panel also affects the system's characteristics. The main error amplifier (MEA) signal is generated using the PI controller. The main bus voltage is measured using a voltage divider to ensure regulation. This value is compared with a previously known constant voltage reference. Suppose the regulation is disrupted due to an error or a voltage difference between the comparator inputs. In that case, this error amplifier circuit generates an error signal according to the proportional gain and integral gain.

This amplified error signal provides a gradually varying current in a ladder like structure to sequentially operated solar panel sections. The difference between the current required by the loads and the current supplied is compensated by the main bus capacitor.

As the number of S3R cells increases, the current per cell will decrease, and current fluctuations in the main bus will decrease, resulting in a more uniform current profile. However, increasing the number of cells does not affect switching delays [2].

The design requirements are given in Table 1. Simulation blocks of the system are shown in Fig. 2. S3R topology operates under bang-bang (hysteresis) control. S3R topology can operate in 3 modes: It can feed the main bus, shunt current to ground, or operate in switching mode to precisely adjust the required power. Each segment of S3R cells contributes to regulation in one of these three modes. Each S3R cell is controlled by signals derived from the error voltages of the main bus interacting with hysteresis comparators. Hysteresis comparators are designed to form a ladder that describes the current state of the system [2]. The circuit diagram of an S3R block is shown in the Fig. 3.

To summarize, S3R has 3 operating modes. These are;

1. When MOSFET is turned off, Solar panel power is transmitted to the load.

2. When MOSFET is turned on, the power of the solar panel is not needed; the generated power is shunted through the MOSFET.

3. When the MOSFET is in switching mode, to precisely adjust the required power.

The diode in the topology prevents reverse current flow from the main bus to the solar panel. In S3R circuits, regulation of the main bus is provided by the MEA signal. When the satellite is exposed to the sun, the S3R circuit charges the battery and disposes of the excess power produced. During eclipse periods, the battery is discharged, and the regulation of the main bus is maintained. Since each load may have different power needs in the satellite electrical power system, it is advantageous for the system to operate independently of each other and to have a modular design.

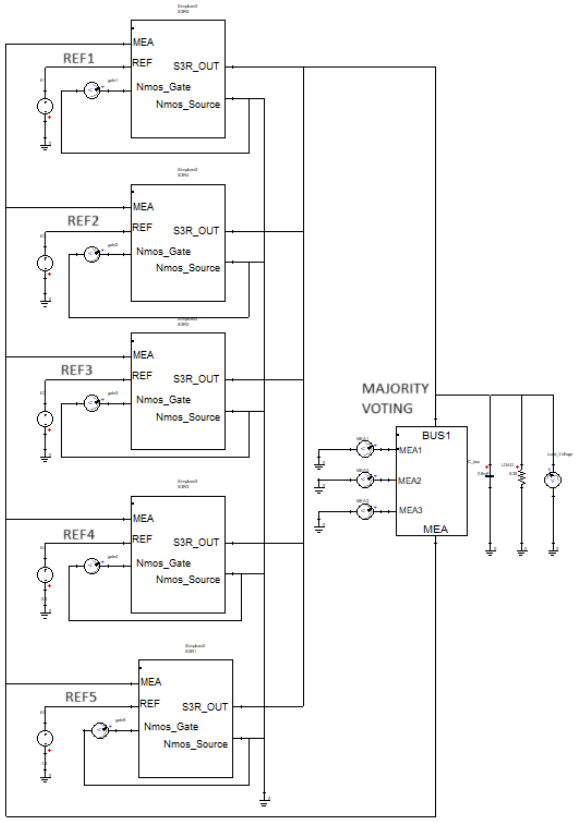

Fig. 2. Simulation blocks of the system

Table 1. Design Requirements

Power	200 W
Bus Voltage (V_{bus})	28 V
Solar Array Sections	1 A x 5
Harness Inductance	30 uH
Parasitic Capacitance	200 nF x 5
Main Bus Voltage Ripple	1%

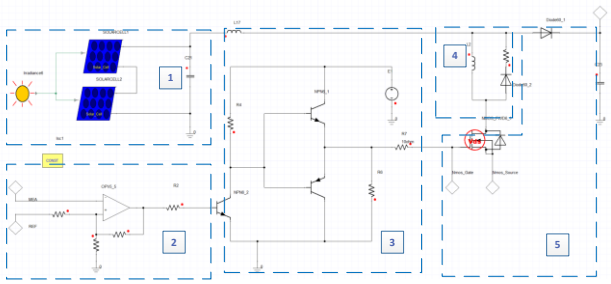

Fig. 3. S3R Section Block; 1-Solar Panel, 2-Hysteresis Comparator, 3-Gate Driver,4-Current Limiter, 5-S3R Cell

2.1. Control Signal Generation

In the majority voting circuit, the control signal is put into three-way voting. The result given by at least two of them is considered correct, and the MEA signal is transmitted to the hysteresis control circuit. Since it is a critical process to balance the produced power with the consumed power and to ensure the regulation of the main bus, and since critical tasks depend on a single control signal, the majority voting circuit has been added to provide protection against single point failure (SPF) [3]. The circuit structure where the MEA signal is generated is shown in Fig 4. The majority voting circuit simulation block is shown in Fig. 5.

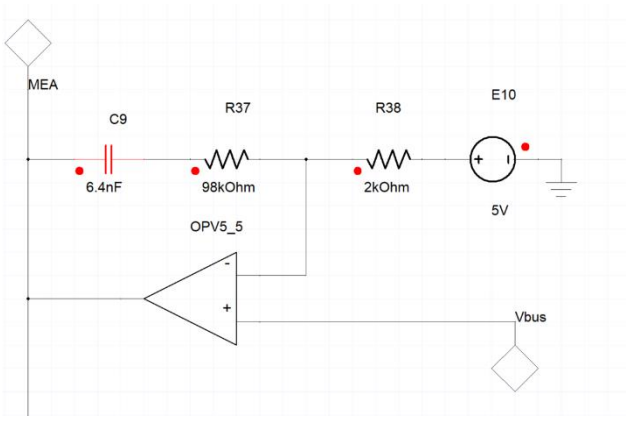

Fig. 4. MEA signal generation

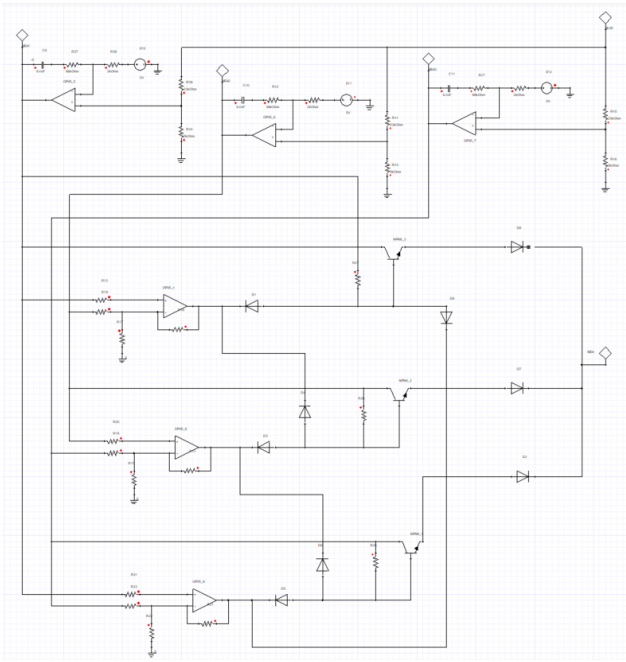

Fig. 5. Majority Voting Circuit[4]

The circuit containing hysteresis and changing its output according to the voltage of the main error amplifier signal in S3R is shown in Fig. 6. This hysteresis range is equal to the difference between the threshold voltages determined when creating the reference voltage.

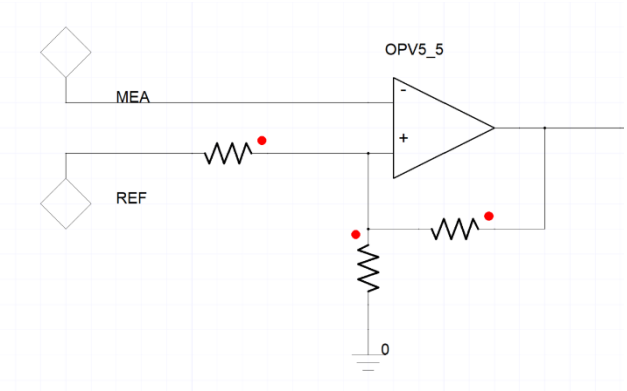

Fig. 6. Hysteresis Comparator

2.2. Current Limiter

While silicon solar panels, which were widely used in the past, had an efficiency of around 18%, a transition was made to multi-junction GaAs-based solar panels due to the need to reach higher power levels. These new-generation solar panels are more resistant to radiation compared to silicon solar panels. The efficiency of GaAs-based solar panels can reach up to 28%, and the transition to higher efficiency solar panels has caused the area of the solar panels to shrink and the volume and weight of the equipment to decrease. It has led to the production of higher powers by occupying less space on the satellite [4].

However, the transition from silicon-based solar panels to GaAs triple junction technology has led to increased parasitic capacitance of solar panels. Since the parasitic capacitance in silicon solar panels is approximately 40nF [5,6] per cell, the solar panel can be modeled as a resistor and diode parallel to the current source, as in Fig. 7. With GaAs solar panels dominating the market, solar panel parasitic capacitance has increased by around five times for the same power ratings [4]. This situation has complicated S3R designs as it increases the current jumps when the MOSFET is in conduction. As the switching frequency increases, the EMC problem arises as the di/dt ratio increases. Under high parasitic capacitance, a low dV/dt ratio will increase the turn-off delay of the MOSFET. Power quality during sudden load change depends only on the performance of the main bus capacitor. Due to delays in the opening or closing times of the MOSFET, deteriorations in the response of the system may be observed. While the delays experienced when the MOSFET is conduction (ON) are caused by the components, the parasitic capacitance of the solar panels causes turn-off delays in the MOSFET. Additionally, if the value of the passive limiting inductor is chosen too large, this will increase turn-off delays. Therefore, current limiting time delay issues should also be considered when designing the system [2]. Turn-on and turn-off delay calculations are given in Equation 1. Turn-on delay is assumed as $1\mu s$ in system design.

$$\tau_{\text{ON}} = \tau_{e^-} = 1\mu s$$
$$\tau_{\text{OFF}} = \tau_{e^-} + \frac{C_{SA}V_{\text{bus}}}{I_{SA}} + 2\sqrt{L_H C_{SA}} = 3.9954.10^{-5} s \quad (1)$$

Active and passive current limiting methods have been used in the literature to reduce the parasitic capacitance effect [4-6]. In the simulation within the scope of this study, the passive current

limiting method shown with number 4 in Fig. 3 was preferred due to its simplicity compared to its active counterpart. The voltage on the inductor will continue to increase as the MOSFET transitions from conduction to cut-off. For this reason, a freewheeling diode was added to the design. The current is limited by a series resistor. The passive current limiter circuit mentioned above is shown in Fig. 8.

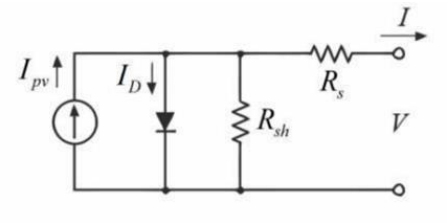

Fig. 7. Solar cell equivalent circuit model

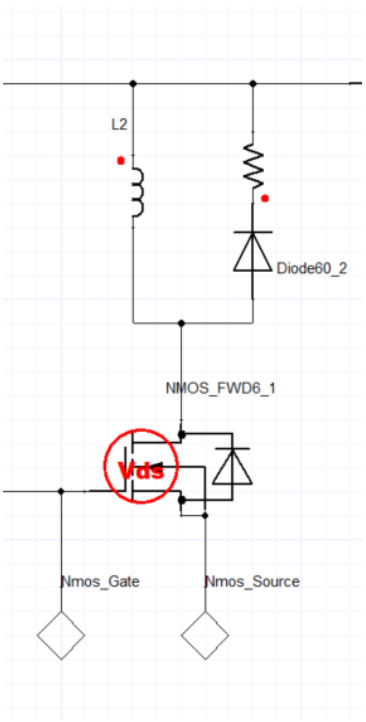

Fig. 8. Passive current limiter with freewheeling diode

In summary, the high parasitic capacitance of GaAs-based solar panels has made the S3R design difficult, as it causes current jumps in the MOSFETs, especially when frequencies are increased. If the parasitic capacitance effect cannot be eliminated, the di/dt ratio during switching will increase, and non-compliance with EMC standards (MIL-STD-461, etc.) will occur.

2.3. Gate Driver Circuit

A totem pole type driver circuit is used to drive the shunt MOSFET in the S3R circuit because the current of the control signal produced by comparing the MEA signal with the reference signal is insufficient to charge/discharge the gate-to-source and gate-to-drain capacitors of the shunt MOSFET. The circuit diagram of the driver circuit is shown in Fig. 9.

When the reference signal is higher than the MEA signal, the NPN type transistor turns on, and the input capacitors of the MOSFET are charged with the 15V supply voltage, and there is no delay in turning on the MOSFET. Both BJTs are controlled with just one pulse. When the reference signal is smaller than the MEA signal, the PNP transistor turns on, and NPN does not turn on. The input capacitance of the pre-charged MOSFET is discharged; thus, the MOSFET turns off. This circuit is also called a push-pull amplifier. Because it can be thought of as pulling or pushing current into the input capacitances of the MOSFET.

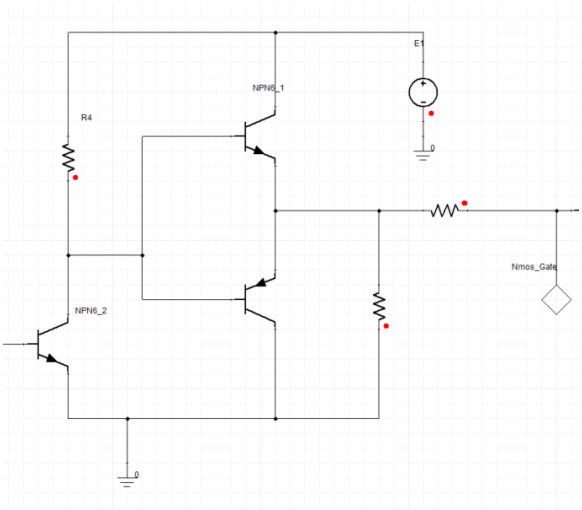

Fig. 9. Gate Driver Circuit

3. Results

Fig. 10 shows the bus voltage and MEA signal. In the 10th ms, when the load increased by 50%, the MEA signal changed, and the main bus did not exceed the 1% voltage fluctuation limit even at a 50% load change, and it was observed that the regulation is preserved.

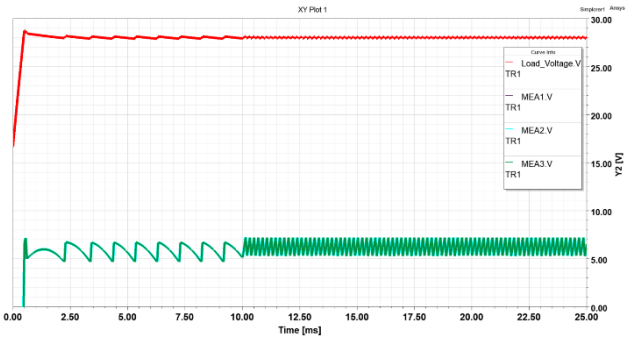

Fig. 10. Main Bus voltage and MEA signal

Fig. 11 shows the current passing through the load. It has been observed that when the load increases by 50%, the current decreases by half.

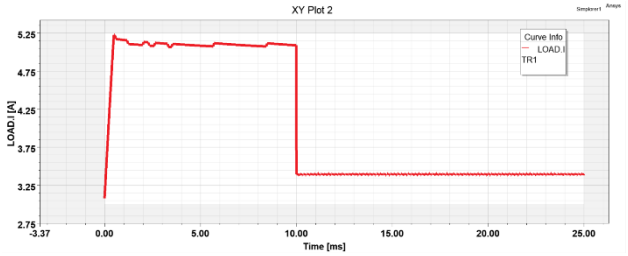

Fig. 11. Load Current

Fig. 12 shows the V_{GS} voltages of the shunt MOSFETs used in the topology. In S3R circuits, only one of the MOSFET operates in switching mode. Others operate in either transmit or shunt mode. It can be seen from Fig. 12 that only the green waveform (gate2.V signal) is in switching mode for the first 10 ms; the others are either in transmit mode or shunt mode. It was observed that when the load changed by 50% after the 10th ms, red waveform (gate4.V signal) went into switching mode instead of gate2.V. The duty cycle of the switching MOSFET is determined by the residual part of a single S3R cell, which is not an exact multiple of the power value for which it is designed. For example, if there is a 60 W power requirement in a 200 W system consisting of five S3R sections with a power of 40 W per each, one S3R section operates in transmission mode, three in shunt mode, and one in switching mode with 50% duty.

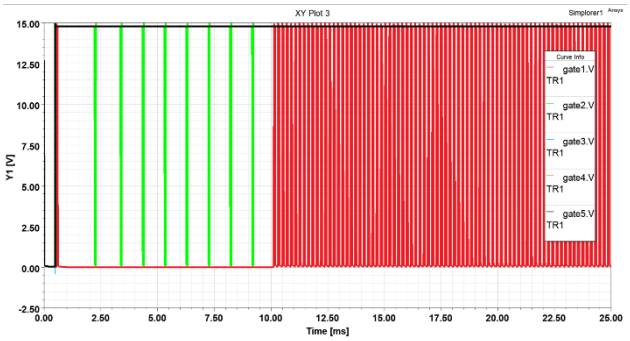

Fig. 12. Switching Voltages of Shunt MOSFETs

4. Conclusions

In this study, an S3R-based solar panel regulation system for a satellite electrical power system has been designed using the DET method, and simulation studies were carried out. In this context, the subcomponents of the solar panel regulator system using S3R topology have been introduced, and a passive current limiting circuit, which has become necessary to be used depending on the developments in panel technology, has been designed. The parasitic capacitance effect was eliminated by adding a passive current limiter. Since it is advantageous to use a simple circuit that uses fewer materials and is less likely to make faults in space applications, a reliable circuit with a low probability of fault was designed by using the majority voting circuit. As a result of the simulation studies, it was observed that the main bus voltage regulation is preserved even under dynamic load change conditions.

5. Acknowledgements

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6. References

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