Design of DAB Converter for Type-2 Charging Infrastructures

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Abstract

One of the crucial interfaces for bidirectional power exchange between two buses with galvanic isolation is the dual active bridge (DAB). This paper presents a design framework tailored to meet the operational needs of a DAB working with type-2 charging infrastructure. It is meticulously crafted to handle the specific demands of an output voltage range from 100V to 1000V. Central to this study is the creation of an extensive dataset, showcasing a variety of suitable switching elements and transformer cores optimized for this voltage spectrum. A detailed analysis of core, copper, and switching losses has been undertaken, examining a myriad of components functioning within the Zero Voltage Switching (ZVS) regime across different voltage and current scenarios. The portrayal of a 500V output voltage stands as a prime exemplar of this study's contributions. Furthermore, the ensuing simulation results are thoroughly compared with outputs from established design methods. This research paves the way for the evolution of sophisticated and efficient charging infrastructures, catering to the burgeoning electric vehicle landscape.

1. Introduction

Bidirectional converters, such as the Dual Active Bridge (DAB) converter, have gained prominence in applications like regenerative motor drives, electric vehicles, and renewable energy systems [1, 2]. The DAB converter offers galvanic isolation and is heralded for its efficiency and bidirectional capabilities, essential for electric vehicle battery management.

Its functionality is contingent upon the phase relationship between its two bridges. By modulating the transformer's transformation ratio, it achieves a balance between buck and boost modes. It is imperative to note that variations from a conversion ratio of 1 result in reactive power losses [3].

To enhance the efficiency of the DAB converter, Phase Shift Modulation (PSM) has been proposed [2], with subsequent studies delving into various nuanced modulation techniques. Innovative modulations, including Extended Phase Shift (EPS), Dual Phase Shift (DPS), Triple Phase Shift (TPS), and Unified Phase Shift (UPS) have been specifically designed to augment the Zero Voltage Switching (ZVS) range and mitigate the RMS current in transformer [3].

Research has demonstrated the efficacy of the Dual Phase Shift (DPS) in reducing RMS inductor current [4]. Further investigations [3] have highlighted challenges, particularly the escalating circulating current when transformer voltage ratios deviate from unity. The Triple Phase Shift (TPS) methodology was introduced to address these nuances.

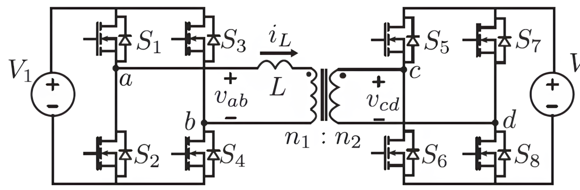

Fig. 1. Topology of Dual Active Bridge converter. There are 2 bridges consisting of 4-switches and a transformer positioned between them

Recent advancements have introduced the switching frequency as an additional degree of freedom alongside the traditional TPS modulation, specifically to minimize core losses in transformers [5]. The quest to minimize switching losses has led to the exploration of strategies like Current Sharing Optimization (CSO). This approach aims to optimize the duty cycles of control signals to switching elements within a closed-loop system [6].

Nevertheless, while many of these strategies are groundbreaking, they necessitate intricate computational methodologies. Although initial design considerations predominantly focus on the power and frequency of the DAB converter, optimizing device-specific parameters is of utmost importance for its overall performance [7]. Past research [6] has largely concentrated on control strategies, revealing a significant gap in dynamic studies concerning the effects of component losses.

In DAB converter design considerations, the primary focus revolves around power delineation, operating frequency, and control modulation. Detailed circuit parameters are subsequently determined, following the consolidation of modulation strategies and operational domains. Objectives concerning total loss or efficiency necessitate a deep understanding of device-specific and magnetics-related parameters, which become clearer post-initial design phases [7]. For DAB converters, optimizing these parameters is crucial for robust operation and steady-state performance [8]. Research documented in [6] suggests a sequential approach to hardware optimization, postulating modulation strategies beforehand. However, a notable gap is observed in literature regarding dynamic studies probing the ramifications of component losses.

The current study articulates a design algorithm predicated on SPS modulation, tailored for an output voltage domain spanning 100V to 1000V. Anchoring this research is a comprehensive dataset featuring an array of switching elements and transformer cores, vetted for compatibility within the aforementioned voltage bandwidth. The exploration evaluates core, copper, and switching losses across diverse components, operating within the ZVS spectrum. Exemplifying the research is a focused assessment at a 500V output, juxtaposing simulation outcomes with algorithmically derived results.

Concentrating on Type-2 charging stations with a nominal 7kW capacity [9], this investigation meticulously conforms to the specifications inherent to the 7kW charging paradigm.

2. Design of DAB Topology

In the converter circuit, a discernible phase shift occurs between the control signals directed to the primary and secondary bridges. The control signals for the diagonal switches of each bridge are coherent in phase, whereas their counterparts exhibit a 180-degree offset. This phase discrepancy is attributable to the transformer's inductive characteristics. Given the inherent lag of the inductive load, by the time current approaches the secondary bridge, a delay is present. The 'leakage inductance' parameter, influenced by the transformer, defines the necessary phase shift for control signals targeted at the lagging bridge.

The converter's performance and efficiency are intrinsically influenced by these control strategies and phase modifications. Analyzing the converter's performance and switching dynamics becomes paramount. With ZVS, a significant reduction in switching losses is achievable, particularly at elevated switching frequencies and under substantial loads. Simulations were conducted across three specific scenarios: initially emphasizing switching losses; subsequently, addressing switch-induced thermal losses; and lastly, a comprehensive assessment factoring in all losses, encompassing those associated with the transformer (both core and copper). The delineation of these scenarios sought to authenticate design codes. Instantaneous current values through the switches and transformer were derived from MATLAB/Simulink, with precise loss tracking, validation, and consistent demonstration of the ZVS advantage intrinsic to the DAB topology.

It is imperative to compute the correlation between leakage inductance and phase shift to ensure the robustness of the design which can be calculated using (1) where, ϕ represents the phase shift in degrees, while f_s denotes the switching frequency. L_r signifies the leakage inductance. V_{in} is the input voltage and V_{out} is the output voltage, while N is equal to $\frac{V_{in}}{V_{out}}$ [10].

$$\phi = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{8 \cdot f_s \cdot L_r \cdot P_{out}}{N \cdot V_{in} \cdot V_{out}}}\right) \tag{1}$$

Upon quantifying the leakage inductance of the constructed transformer, one can ascertain the requisite phase shift. Conversely, having established the magnitude of the phase shift, it becomes feasible to compute the necessary leakage inductance. In addition, the minimum output capacitance value (for minimum loss) required to eliminate the fluctuation in the output voltage is calculated (2) where C_{out} represents the output capacitance. D is the phase shift rate, and it equals to *phase shift/180* while DV_o is voltage fluctuation V_{max} - V_{min}.

$$C_{out} = V_{in} \cdot D^2 \cdot \left(\frac{1 - D + \frac{D^2}{4}}{4 \cdot L_r \cdot n \cdot D \cdot V_o \cdot f_s^2}\right) \tag{2}$$

In design of the DAB converter, mathematical modeling was conducted to estimate switching losses, transformer copper and core losses, as well as thermal rise within the transformer. MOSFETs have been considered as the switching elements, and an EE-type ferromagnetic core has been envisaged for the transformer. The winding wire to be used has been calculated and integrated into the estimation of copper losses. A database of suitable MOSFETs and transformer cores has been compiled for design selection.

2.1. Switching Loss Calculation

Switching losses have been analyzed under four main categories, and each loss has been calculated separately. These losses are considered as conduction, switching, dead time, and gate charge losses [11]. The equations for conduction loss can be calculated as depicted in (3)-(4).

$$P_{ON\text{-}H} = I_o^2 \cdot R_{ON\text{-}H} \cdot \frac{V_{in}}{V_{out}} \tag{3}$$

$$P_{ON\text{-}L} = I_o^2 \cdot R_{ON\text{-}L} \cdot \left(1 - \frac{V_{in}}{V_{out}}\right) \tag{4}$$

Calculations have been made separately for the high side and low side MOSFETs. Switching loss, on the other hand, has been calculated for the high side MOSFETs only in both bridges as represented in (5).

$$P_{SW\text{-}H} = \frac{1}{2} \cdot V_{in} \cdot I_o \cdot (t_r + t_f) \cdot f_s \tag{5}$$

Gate charge loss refers to the power dissipation resulting from charging the MOSFET gate. This loss is contingent upon the electric charge of the gate (or the gate capacitance) for both the high-side and low-side MOSFETs [11]. This loss can be calculated as indicated in (6).

$$P_G = (Q_{g\text{-}H} + Q_{g\text{-}L}) \cdot V_{gs} \cdot f_s \tag{6}$$

while the high side and low side MOSFETs simultaneously conduct, they cause a brief short circuit between the source and ground, resulting in a dead time loss. This loss is calculated as depicted in (7).

$$P_{dead} = V_{sd} \cdot I_o \cdot (t_r + t_f) \cdot f_s \tag{7}$$

2.2. Design of Transformer

In the process of transformer design, the initial step involved calculating the area product of the transformer core. Subsequently, the required winding numbers for the primary and secondary coils were determined, followed by the specification of conductor cross-sectional areas based on the currents passing through the windings. Finally, calculations for copper and core losses, as well as temperature rise, were conducted based on these parameters. The area product of the transformer to be used must be greater than or equal to the calculated value [12, 13]. The area products are calculated by (8)-(11), with variations accounted for based on temperature increases. Where K_v represents the waveform factor, which is equated to 4 for a square wave. K_u stands for the window utilization factor. P_t symbolizes the aggregate of input and output powers. J signifies the current density, whereas pw pertains to the resistivity of copper at its peak temperature. The constant K_t indicates the thermal resistance. Additionally, certain constants are specified as $a_2 = 0.00393$, $ka = 40$, $kw = 10$, $K_f = 0.95$ (applicable to laminated cores), and $hc = 10$. B_m represents the maximum magnetic flux density that the core can support before reaching saturation.

$$req\_ap = \frac{P_t}{K_v \cdot B_m \cdot f_s \cdot K_u \cdot J} \tag{8}$$

$$pw = 1.72 \cdot 10^{-8} \left(1 + a_2(T_{max} - 20)\right) \tag{9}$$

$$K_t = \sqrt{\frac{hc \cdot ka}{pw \cdot kw}} \tag{10}$$

$$req\_ap\_T = \frac{\sqrt{2} \cdot Pt}{K_v \cdot B_m \cdot f_s \cdot K_f \cdot K_t \sqrt{K_u \cdot \Delta T}} \tag{11}$$

At the saturation point, the magnetic flux density of the core can no longer increase, which could adversely affect the performance of the transformer. This value can be obtained from the B-H curve in the datasheet of the core, or it may be a ratio such as 50%-60% of the B_{sat} value for ferrite materials.

After the area product was calculated and the winding numbers for both primary and secondary were determined, the length and width of the transformer core window should also be considered to fit the windings. In this context, the areas of the windings for both primary and secondary, as well as their lengths depending on the number of windings, were calculated. Accordingly, a core was selected from the prepared database. Subsequently, primary and secondary number of turns are calculated in (12)-(13) [12] where A_e is the effective cross-sectional area. After the number of turns was calculated, the gauge number of the Litz wire to be used was calculated.

$$N_p = \frac{V_{in}}{K_v \cdot f_s \cdot B_m \cdot A_e} \tag{12}$$

$$N_s = N_p \cdot \frac{V_{out}}{V_{in}} \tag{13}$$

Due to the presence of the proximity effect and the skin effect, multi-stranded Litz wire should be used for high frequency operation [13]. The radius of each strand of Litz wire must be lesser than the skin depth parameter [14] which is calculated by (14).

$$\delta = \frac{1}{\sqrt{\pi \cdot f_s \cdot \mu \cdot \sigma}} \tag{14}$$

where μ is permeability of copper, and σ is conductivity of copper. After each single wire diameter was found, the number of Litz can be calculated according to total winding diameter. The radius of total winding is calculated as depicted in (15).

$$Radius \geq \sqrt{\frac{I_{rms}}{J \cdot \pi}} \tag{15}$$

Here, the smallest unit wire from the AWG table can be directly selected for each individual Litz wire for ease of production in real environment. Here, AWG 26 was selected for a single strand of each Litz wire, and the number of strands was calculated as 43 for the primary and 36 for the secondary.

After the number and diameters of the windings are determined, the R_{ac} parameter can be found to calculate in (16)-(17) to calculate copper loss [13].

$$R_{dc} = \frac{N \cdot MLT \cdot \frac{1}{\sigma}}{\pi \cdot r_s^2} \cdot \frac{1}{number\_of\_Litz} \tag{16}$$

$$R_{ac} = R_{dc} \cdot \left[1 + \left(\frac{r_s}{\delta}\right)^4 \cdot \frac{1}{48 + 0.8 \cdot \left(\frac{r_s}{\delta}\right)^4}\right] \tag{17}$$

Finally, core and copper losses were calculated in (18)-(19) where C_m, α and β are constants and can be provided in the datasheet. The term Tr_v represents the volume of the core, while MLT stands for mean length turn. Additionally, rs denotes the radius of single wire, while R_{dc} and R_{ac} refer to DC and AC resistances respectively.

$$P_{core} = C_m \cdot f_s^{\alpha} \cdot B_{sweep}^{\beta} \cdot Tr_V \tag{18}$$

$$P_{copper} = I_{rms}^2 \cdot R_{ac} \tag{19}$$

Besides these, the increase in the operating temperature of the transformer was calculated. To perform this calculation, it is necessary to determine the thermal resistance (R_{thet}). The temperature increase in the transformer can be calculated according to (20)-(22) [15].

$$R_{thet} = (53 \cdot Tr_V \cdot 10^6)^{-0.54} \tag{20}$$

$$P_{total} = P_{core} + P_{copper} \tag{21}$$

$$\Delta T = R_{thet} \cdot P_{total} \tag{22}$$

In the simulation environment, when calculating the core loss, the software references the L_m (magnetizing inductance) parameter calculated in (23). In the designed transformer, 0.5mm air-gap has been introduced, and the L_m value was determined accordingly. The A_l value (inductance per turn) used for this calculation was selected based on the corresponding value for the specified air gap in the core datasheet [16]. Since the utilized air gap can significantly reduce the L_m value, a magnetizing inductance value is required to an extent where ZVS observations can also be made [17].

$$L_m = N \cdot Al \tag{23}$$

3. Results and Discussions

The relevant parameters of the simulated topology are listed in Table 1.

Table 1. Converter specifications

Total Output Power (Pout)	7kW
Input Voltage (Vin)	400V
Output Voltage (Vout)	500V
Switching Frequency (fs)	100kHz
Phase Shift (ϕ)	50°

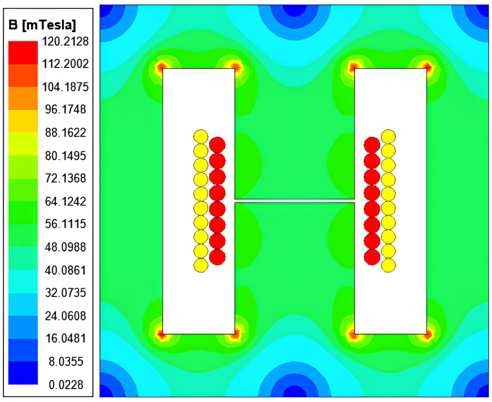

Fig. 2. Magnetic flux density of transformer

3.1. Modelling of Transformer

Modeling of the transformer commenced within the PEmag module of the ANSYS. Guided by the calculated parameters, the preferred transformer core was selected within the software, along with previously computed number of windings for both the primary and secondary. Subsequently, the developed model was transferred to ANSYS for further analysis. Both transient and electrostatic analyses were conducted in this environment. The transient analysis was employed to observe core loss and copper loss, whereas the electrostatic analysis was used to scrutinize parasitic capacitance values. The selected transformer core for simulation is 3C95-E65/32/27. The transformer designed has been transferred to Ansys. Subsequently, magnetic flux distribution is shown in Fig. 2.

Studies in the literature suggest that the power losses caused by the proximity of windings and the inter-winding capacitance can be mitigated by employing an interleaved winding configuration. Interleaving windings can also lead to a reduction in leakage inductance. Noteworthy effects of high-frequency operation include the fringing effect observed near the air-gap, as well as the proximity effects both within individual windings (intra-winding) and between separate windings (inter-winding) [18].

3.2. Simulation Study

The assessment of power losses in this study involved the individual simulation of switching, transformer, and total losses. Subsequently, the holistic evaluation encompassed total power loss, transformer input and output currents, converter output power, and the achievement of ZVS. In line with these simulations, parasitic capacitance values, as previously determined, were integrated into the simulation framework(Fig. 3). For these simulations, the selected switching devices were the STW88N65M5-4. To enhance the optimization of switching losses, diverse parameters outlined in the respective MOSFET's datasheet were precisely defined within the 'Device database editor.' Furthermore, the drain-to-source current and voltage characteristics were established (Fig. 4).

Simulation outputs, include input and output voltages, ZVS condition for first MOSFET, and the output current and voltage are depicted in Fig. 5. Finally, simulation results and mathematical calculations are compared in Table 2 as a result of the study. In addition to these studies, it has been observed that an additional power loss of 98.63W occurs when the ambient temperature is

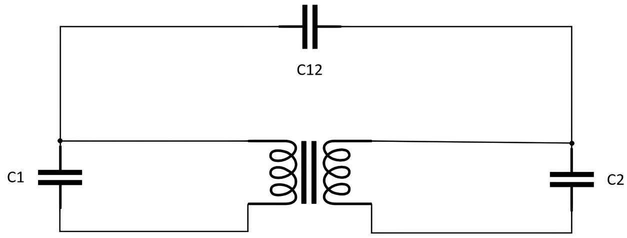

Fig. 3. Adding calculated parasitic capacitances to the simulation [19]

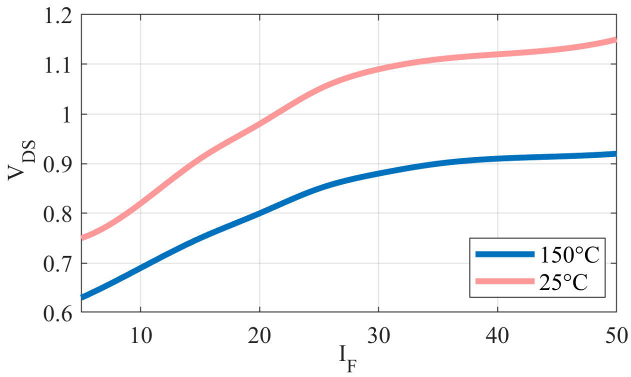

Fig. 4. Source to drain voltage and current curves taken from datasheet

Table 2. Comparision of analytical and simulation results

	Numerical	Simulations
Core Loss [W]	4.85	5.1
Copper Loss [W]	4.25	4.55
Switching Loss [W]	69.296	72.8

set to 40 degrees (taking into account the subsequent temperature rises with no cooling).In addition to switching losses, extra loss in the transformer were found to be 5.7W in PSIM, and this result agrees with Ansys results.

4. Conclusion

In this paper, as it is observed that the Type-2 infrastructure is notably common considering the prevalence and cost factors, a design for a 7kW Dual Active Bridge (DAB) converter, capable of generating an output voltage ranging from 100V to 1000V for utilization in these charging stations, has been proffered to provide significant convenience in determining circuit parameters for need-oriented design criteria. Additionally, an exhaustive analysis of losses incurred by this converter has been conducted. To facilitate this study, datasets encompassing suitable MOSFETs and transformer cores capable of operation within this specified voltage range have been compiled. These losses have been independently computed through both analytical and simulation methodologies.

Furthermore, the ZVS occurrence within the designed converter was noted, with the correlation between leakage inductance and phase shift elucidated. Necessary capacitor values and transformer design parameters were detailed. Simulation efforts initially analyzed switching losses, then studied temperature-induced variations. Ultimately, a comprehensive analysis of all losses, in-

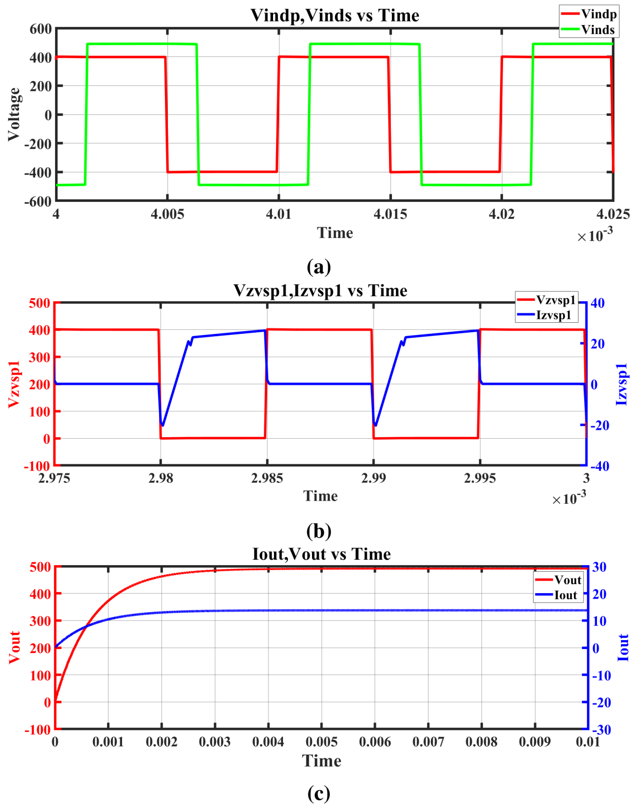

Fig. 5. Input and Output voltages of transformer, current and voltage waveforms on the first MOSFET, and output current and voltage respectively.

cluding transformer losses, was presented with mathematical visualization for clarity.

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5. References

[1] G. G. Oggier and M. Ordonez, "High-efficiency dab converter using switching sequences and burst mode," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2069–2082, Mar 2016.

[2] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation strategy to operate the dual active bridge dc-dc converter under soft switching in the whole operating range," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1228–1236, Apr 2011.

[3] Y. Deng, S. Yin, J. Chen, and W. Song, "A comprehensive steady-state performance optimization method of dual active bridge dc-dc converters based onwith triple-phase-shift modulation," in *2022 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Nov 2022, p. 221–225.

[4] W. Han, R. Ma, Q. Liu, and L. Corradini, "A conduction losses optimization strategy for dab converters in wide voltage range," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Oct 2016, pp. 2445–2451.

[5] H. Zhang, X. Tong, J. Yin, and F. Blaabjerg, "Neural network-aided 4-df global efficiency optimal control for the dab converter based on the comprehensive loss model," *Energy*, vol. 262, p. 125448, Jan 2023.

[6] N. Hou, W. Song, and M. Wu, "Minimum-current-stress scheme of dual active bridge dc-dc converter with unified-phase-shift control," *IEEE Trans. Power Electron.*, pp. 1–1, 2016.

[7] D. Das and K. Basu, "Optimal design of a dual-active-bridge dc–dc converter," vol. 68, no. 12, Dec 2021, pp. 12 034–12 045.

[8] A. Rodriguez Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a dual active bridge for bidirectional dc/dc conversion," in *2010 IEEE Energy Conversion Congress and Exposition*, Sep 2010, p. 1129–1135.

[9] SaveMoneyCutCarbon. (2023, 09) Home electric vehicle charging: Ev cables. [Online]. Available: https://www.savemoneycutcarbon.com/category/home-electric-vehicle-charging/ev-cables/

[10] L. Song, H. Ramakrishnan, N. N. Kumar, and M. Bhardwaj, "Bidirectional, dual active bridge reference design for level 3 electric vehicle charging stations," Texas Instruments, Tech. Rep., Jun 2019.

[11] "Calculation of power loss (synchronous)," ROHM Semiconductor, Tech. Rep. Application Report AEK59-D1-0065–2, Oct 2016.

[12] E. Iuravin, "Transformer design for dual active bridge converter," Ph.D. dissertation, Miami University, 2018.

[13] W. H. Wölfle and W. G. Hurley, *Transformers and Inductors for Power Electronics Theory, Design and Applications*. Wiley Publication, 2013.

[14] S. Dey, S. S. Chakraborty, S. Singh, and K. Hatua, "Design of high frequency transformer for a dual active bridge (dab) converter," in *2022 IEEE Global Conference on Computing, Power and Communication Technologies (GlobConPT)*, Sep 2022, p. 1–6.

[15] E-Magnetica. (2023, 09) Thermal resistance. [Online]. Available: https://www.e-magnetica.pl/doku.php/thermal_resistance

[16] A. Lordoglu, M. O. Gulbahce, D. A. Kocabas, and S. Dusmez, "A holistic design optimization method for llc converters in light electric vehicle chargers," *IEEE Trans. Transp. Electrification*, pp. 1–1, 2023.

[17] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *IEEE Transactions on Industry Applications*, vol. 28, no. 6, pp. 1294–1301, Nov.-Dec. 1992.

[18] A. Lordoglu, M. O. Gulbahce, D. A. Kocabas, and S. Dusmez, "A new optimization method for gapped and distributed core magnetics in llc converter," *IEEE Access*, vol. 11, pp. 14 061–14 072, 2023.

[19] A. C. Güngör, A. Lordoglu, M. O. Gülbahçe, and D. A. Kocabaş, "Llc rezonans dönüştürücünün parazitik elemanlarının dahil edildiği yüksek doğruluklu benzetim modeli," in *Elektrik, Elektronik ve Biyomedikal Mühendisliği Konferansı, ELECO 2022*, 2022.