Design and Implementation of a GaN Power IC Based High Frequency Class-D Power Amplifier

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Abstract

In this paper, we present an approach to utilize recently emerged GaN Power Integrated Circuits (IC) in a high frequency Class-D power amplifier design. Although these ICs simplifies the design and implementation of power converters, there are still crucial considerations that should be followed when it comes to high switching frequencies. GaN FET technology offers lower $R_{DS,ON}$ values and faster switching characteristics, which results in lower losses in conversion. However, research is needed to make them widespread in the industry. In this study, we utilized two Half-Bridge GaN power ICs for a Class-D power amplifier with 1 MHz of switching frequency, 100 kHz of output frequency, 48 VDC of input voltage and 40W of output power. Throughout the paper, we present a clear step by step guideline for this design, considerations for its practical implementation and experimental results showing the feasibility of these GaN ICs in high frequency applications.

1. Introduction

THERE are many applications where an electrical device needs to be driven with high frequencies. For example, this device may be a piezoelectric acoustic transducer for an underwater SONAR application with a high frequency spectrum such as sub-MHz. Depending on the transducer characteristics and the platform where this system is going to be built, there will be cost, size, weight, efficiency, Total Harmonic Distortion (THD) and linearity requirements.

Linear amplifiers provide lower THD and higher linearity comparing with switching amplifiers such as Class-D. But for high power applications, low efficiencies of linear amplifiers cause large sizes and weights which can not be tolerable for most of the systems.

Basic block diagram of Class-D power amplifier is depicted in Figure 1. It provides higher efficiencies comparing with linear counterparts [1, 2]. However, its output voltage waveform contains harmonics because of its non-ideal switching behavior. One of the causes for this non-ideality is that there are dead-times between ON and OFF instants of complementary switches which causes unwanted harmonics.

These dead-times are large enough to distort the resulting signal. The enforcing reason for these large dead-times is to prevent shoot throughs. Because, the switches have capacitive behaviors, i.e., it takes time for them to turn ON and OFF. If a switch turns ON without waiting its complementary switch to turn OFF, they both cause a shoot-through and hence large currents

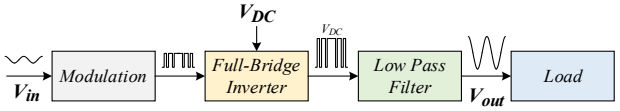


Fig. 1. Basic block diagram of Class-D power amplifier

flow through this circuit. If this current can not be cut off in a short enough time, the circuit will be damaged. So, for these topologies, dead-times are inevitable. Although dead-times provide a safe operation by preventing shoot-throughs, any other intolerable high currents should be detected for further protection. In other words, there has to be also Over Current Protection (OCP).

When it comes to limits of the nature of the switches, to increase the performance in terms of efficiency and THD, one has to look for faster switches which can turn ON and OFF in shorter period of times. Thanks to the advances in semiconductor technology there are wide-bandgap semiconductor switches which make it possible to decrease these dead-times. Especially, Gallium Nitride (GaN) Field Effect Transistors (FET) can turn ON and OFF very rapidly comparing with Silicon (Si) and Silicon Carbide (SiC) alternatives [3]. So, GaN FETs are highly promising for high frequency switching applications. In this study, we specifically examine their applicability to a Class-D power amplifier with high switching frequency.

GaN FETs can be found in the forms of discrete packages and gate driver integrated packages. It is obvious that for industrial applications gate driver integrated GaN FETs are more preferable due to easy, fast and reliable design [4, 5]. In this study, we focus on gate driver integrated solutions. There are a few commercial GaN Integrated Circuits (IC) which contains both the GaN FET and its gate driver together in the same package. Table 1 compares these well-known GaN Power ICs. There are packages with single GaN FET and also with double GaN FET configured as a Half-Bridge. Although single packages are advantageous in terms of flexibility and replaceability with alternatives, there are a few important reasons for us to select Half-Bridge modules in this study. One of the most crucial reason is that Half-Bridge modules helps for lowering the inductance of inter connections between high side and low side FETs, which eliminates high voltage ringing, in mid-points of the bridge circuit, caused by high rate of change of current. Secondly, it can be shown that, the Figure of Merit (FOM) for Half-Bridge configuration is lower when we compare Navitas NV6169 (Single) and Navitas NV6269C (Half-Bridge) due to the its lower output charge.

Shoot-Through Protection (STP) is one of the critical features

Table 1. Comparison for Single (S) and Half Bridge (HB) configurated commercial GaN ICs.
Abbreviations: Switching Frequency (F_{SW}), Propagation (Prop.), Drain-Source Voltage (V_{DS}), Figure Of Merit (FOM), Over Current Protection (OCP), Current Sense (CS), Over Temperature Protection (OTP) and Shoot-Through Protection (STP)

MFN PN	S / HB	Max. F_{SW} (MHz)	ON Prop. Delay (ns)	OFF Prop. Delay (ns)	Rise Time (ns)	Fall Time (ns)	V_{DS} (V)	I_D (A)	$R_{DS.ON}$ (mΩ)	Q_{OSS} (nC)	FOM	OCP	CS	OTP	STP	Temp. Range (ºC)
EPC EPC9089	S	7	2,7	17	2,7	5,5	160	10	32	24	768	-	-	-	-	-40 ~ +150
Navitas NV6138C	S	2	30	24	7	5,5	700	8,6	120	20,5	2460	+	+	+	-	-55 ~ +150
Navitas NV6169	S	2	22	13	6	14	650	24	45	75	3375	+	+	+	-	-55 ~ +150
Navitas NV6269C	HB	2	65	50	16	14	650	14	70	37,5	2625	+	+	+	+	-55 ~ +150
EPC EPC90120	HB	3	30	30			80	15	10	26	260	-	-	-	-	-40 ~ +125
EPC EPC90147	HB	3	36	36	3	3	100	35	5,2	29	150,8	-	-	-	-	-40 ~ +150
EPC EPC90152	HB	3	20	20	3	3	100	15	8,7	15	130,5	-	-	-	-	-40 ~ +150
TI LMG5200 EVM-02	HB	10	30	30			80	10	15	21	315	-	-	-	-	-40 ~ +125
TI LMG2100 EVM-078	HB	10	35	35			100	35	4,4	55	242	-	-	-	-	-40 ~ +150

of a gate drive circuit. There are many researchers investigating the STP for GaN FETs. Because of very short ON and OFF times of these GaN FETs, it is not straightforward to cut off the current on GaN FET in shoot-through instants. In Table 1, the only HB power IC providing STP effectively is Navitas NV6269C and this is the main reason why we selected this specific IC for this study.

These modules or so-called Power ICs are utilized in lower frequencies in most of the researches because the main focus of these studies is to increase the efficiency by decreasing the switching losses. Taking this fact into consideration, the main contribution of this paper is that it gives a clear guideline for the utilization of these GaN based half-bridge integrated circuits in a practical high frequency Class-D power amplifier.

Throughout the paper, for a high frequency Class-D power amplifier, we presented the design details in Section II, considerations in practical implementation in Section III, experimental verification of the design in Section IV and finally we concluded the paper with a conclusion. We hope that this paper serves as a guideline to design engineers and researchers in utilizing GaN Power ICs in high frequency power electronics applications.

2. Design of GaN Based Class-D Power Amplifier

The Class-D power amplifier consists of a modulation stage, a DC link capacitor, a Full-Bridge inverter, an output filter and a load. Figure 1 shows the basic block diagram of Class-D power amplifier. The modulation stage produces Sinusoidal Pulse Width Modulation (SPWM) to drive the Full-Bridge stage. In the Full-Bridge stage, the high frequency signals are amplified by switching a DC voltage according to the related signals modulation. The filter block attenuates the high frequency components and provides a fundamental signal with low THD.

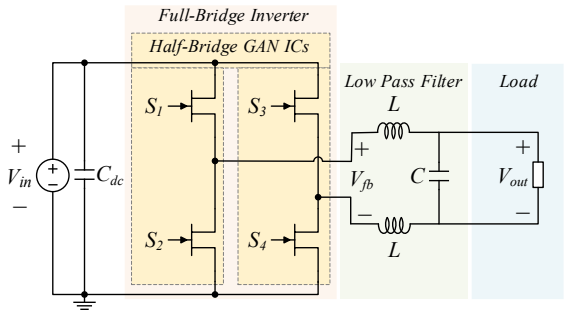


Fig. 2. Detailed circuit diagram for GaN FET based Class-D power amplifier

The amplifier must provide low distortion on the output signal to correctly convert the electrical signal to acoustic signal.

Recent developments of semiconductor technology especially GaN FETs have facilitated Class-D amplifier designs that are more compact, higher power density, improved efficiency and lower THD [6, 7]. All the design steps related to Class-D amplifier are given in the following subsections.

2.1. Full-Bridge Inverter Design

The Full-Bridge design is an essential part of the Class-D amplifier. Low leakage inductance, short rise and fall times of FETs are critical requirement in high frequency amplifier. Two pieces of NV6269C, Navitas integrated Half-Bridge GaN FET Power ICs were used in Full-Bridge design. It has low inductance at the connection point of two GaN FETs, high frequency capability, current sensing, integrated with gate drivers and protections. Figure 2 illustrates a Full-Bridge Class-D power amplifier with four pieces of GaN FETs which is satisfied by utilizing two Half-Bridge modules.

Design parameters of Class-D power amplifier are defined in Table 2. Switching frequency is selected 1 MHz to resulting THD of the output signal. A 100 kHz sinusoidal signal with low THD can be used in applications such as piezoelectric sensor, SONAR system, ultrasonic equipment and related applications.

Table 2. Design parameters of Class-D power amplifier

Parameters	Value
Switching frequency	1 MHz
Fundamental frequency	100 kHz
Output load impedance	24 Ω
Output power	40W
Supply voltage	48V
Total harmonic distortion (THD, theoretical)	< 3%
Efficiency (theoretical)	> 90%

2.2. DC-Link Capacitor Design

At the high-frequency inverters, the DC-Link capacitor serves a pivotal function in ensuring stable operation. Aluminum Electrolytic capacitors offer higher capacitance and energy densities value per unit volume compared to ceramic, tantalum and film capacitors [9, 10]. However, since they have disadvantages in terms of high ESR and ESL, it is recommended to parallel many of them for lower ripple. The following equation (1) was used to determine the DC-Link capacitance value.

$$C_{dc} = \frac{P \cdot K}{V_{dc}^2 \cdot fsw \cdot \Delta V} \tag{1}$$

In the formulation (1), "*K"* is a constant that usually taken as a value between 1 and 2 and is chosen depending on the desired voltage ripple level. In this study "*K"* is selected 1.5. In similar applications, accurate capacitor calculation and careful selection are essential for system reliability. Key factors to consider include temperature, voltage range, expected lifetime, and achieving a high capacitance-to-volume ratio. As standard 2 x 47uF electrolytic capacitors selected and paralleled.

2.3. Output Filter Design

Midpoint of the Class-D needs a low-pass filter to suppress high-frequency harmonic components to obtain lower THD on output sine wave. Quality factor (Q) and cut-off frequency have a determining role in the Butterworth second-order filter. While critically and over damped frequency responses are more suitable in the audio industry, this study focused more on underwater acoustics. For this reason, Q = 1.2 was chosen to aim for the system to work at underdamping. To illustrate the Type-1 filter that single-ended equivalent circuit depicted as shown in Fig. 3.

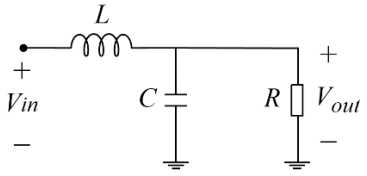


Fig. 3. Single-ended equivalent circuit of the filter stage

The Q factor for a parallel RLC circuit:

$$Q = R \cdot \sqrt{\frac{C}{L}} \tag{2}$$

And the cut-off frequency equations:

$$f_0 = \frac{\omega_0}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \tag{3}$$

$$\omega_0 = \frac{1}{\sqrt{L \cdot C}} \tag{4}$$

Using (2) and (4), calculated parameter values L = 15.9µH and C = 80nF with decided resistive load R = 24 Ω. However, standard closest component values were selected. These are 15µH Würth's shielded power inductor and 83 nF Kemet's PHE 850 and 845 series capacitors.

2.4. PWM Generator Design

STM32H563ZI MCU was used to generate SPWM for GAN FETs. STM32H563ZI MCU has high performance Arm Cortex 32-bit core, 250 MHz clock frequency, 2 MB flash, 640 KB RAM and floating-point unit (FPU). The full-bridge was driven by bipolar and unipolar SPWM signals at 1 MHz switching frequency.

An appropriate dead time must be provided to prevent shoot-through in GAN FETs and improve THD of output signal with suitable dead time. When low side GAN FET is turn-off, dead time (t_{dt}) must be higher than the off transient delay time ($t_{d,off}$) and the transient time ($t_{sw,off}$) [8]. Based on mathematical calculations and controlled measurements on the experimental setup, a dead time of 44 ns was implemented.

$$t_{dt} = t_{d,off} + t_{sw,off} \tag{5}$$

3. Practical Implementation

An application study was carried out in the laboratory for this circuit which was examined in detail in simulation environment with mathematical calculation. Some issues that have no significant impact at relatively lower frequency studies have become problems that need to be focused on separately in our study.

3.1. Hardware Setup Considerations

The midpoint of the full bridge converter is the most critical node where high-frequency components are amplified and radiated into the environment. Line from this node to low-pass filter inductor should be kept as short as possible. If it is not satisfied, effect of the transmission line will cause grounding bounce and EMI issues due to dV/dt and dI/dt.

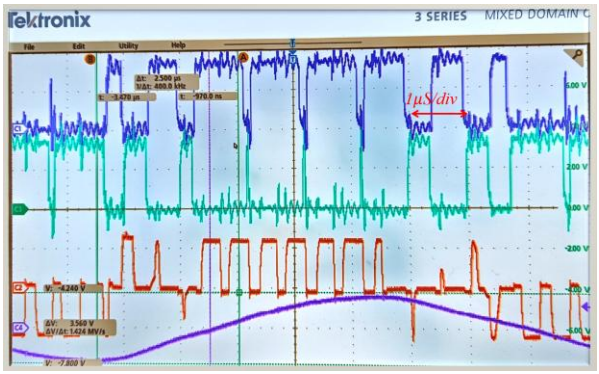
Distance from mid-node to low-pass filter inductor has been changed to observe effect of the power loop inductance. In the first established assembled circuit, distance from mid-node to filter inductor measured as 2.5cm, while in the improved version it has been reduced to a value close to zero. The power loop inductance level is highly effective factor on voltage overshoots, spikes, power losses and EMI [11]. Both gate loops and power loops must minimize in converter circuits.

Shown at a study [12], 3-inch ground lead of passive oscilloscope probe collected any radiation from the surrounding area, while acting as an antenna. It is highlighted that being small-length of passive probe's lead is important issue when measured fast signals.

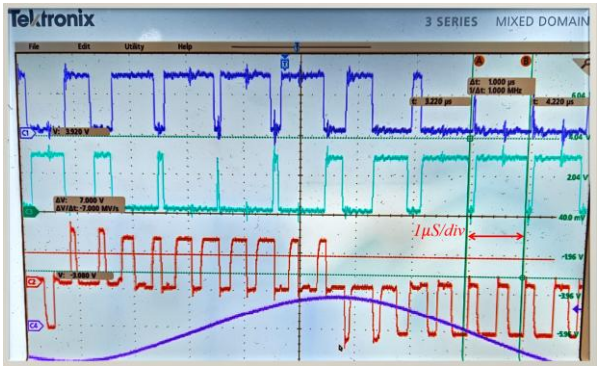
Another important issue is transfer of PWM signals generated by the STM32 to the hardware stage for gate driving. While using normal jumper cable in the first stage, it was later developed to coaxial cable suitable for header pins and GaN modules.

In addition to these, for minimizing physical size of the loop to reduce parasitic inductance, the DC-Link capacitor place in input side is positioned as close to Half-Bridge drain and source pins. Also, by doing this midpoint stabilization is ensured since every distance between this capacitor and inverter Vin will cause a voltage drop due to resistive and inductive components in DC bus.

As a result of the improvements made, it was observed that false FET switching decreased, overall switching performance increased while loss of efficiency causes of the ringing and other noises were inhibited. Scope photos after the result of the improvements shown in Fig. 4.



(a)



(b)

Fig. 4. Experimental results showing the impact on one leg (HS&LS, blue&green) PWM signals (mid-node&output, red&purple) *(a)* before improvements and *(b)* after

3.2. PWM Generator Software Considerations

Using STM32H563ZI MCU is generated bipolar and unipolar 1 MHz SPWM signals. First, the duty cycle values were calculated in every switching frequency by using function of sinf() and comparing the results with the period. Although the timer clock frequency is 250 MHz, SPWM in the desired frequency could not be generated due to insufficient time for computing the sine function. So, SPWM was generated by using look-up table (LUT). If an MCU with a 480MHz clock frequency is used, the desired sinusoidal frequency can be generated at 1 MHz switching frequency.

Up/down/up-down counters can be used to produce PWM with the desired frequency and duty cycle value when generating PWM with an MCU. Different counters can be used to generate bipolar SPWM but up-down counter must be used for unipolar SPWM. If up or down counter are used in unipolar SPWM, a unipolar signal can be generated but the effective frequency of the generated signal is same with bipolar signal. So, the unipolar SPWM signal is not generated effectively and a higher THD on output signal is observed.

4. Experimental Results

The experimental setup was implemented and observed on oscilloscope. The prototype is shown in figure 5. HV DC input and Vcc ic supply pins are connected to two isolated power supply via twisted pair wires. SPWM signals generated by STM32 board connected converter's power stage using coaxial cables. In order to design a prototype practically, two gan module combined and assembled on the pertinax card and then connected the resistive load which mounted heatsink.

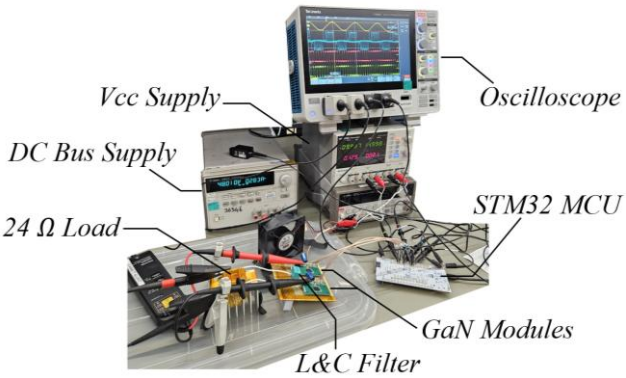


Fig. 5. Experimental prototype of Class-D

Figures 6 and 7 show the oscilloscope capture of the output voltage waveform under modulation index at M=0.93. There are two main PWM switching techniques known as AD and BD, also known as respectively bipolar and unipolar switching.

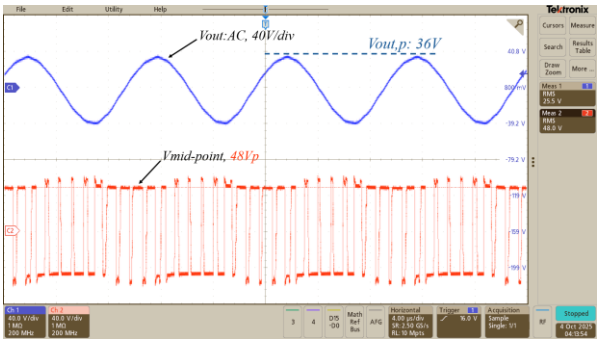


Fig. 6. Experimental AD switching waveform of the full-bridge midpoint (red) and output sine (blue)

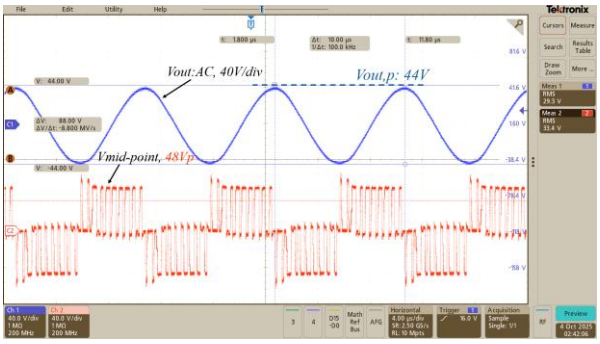
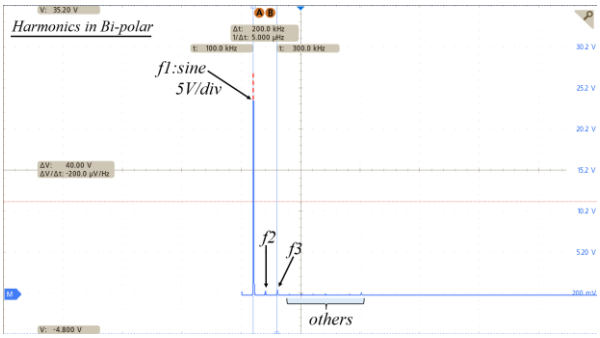
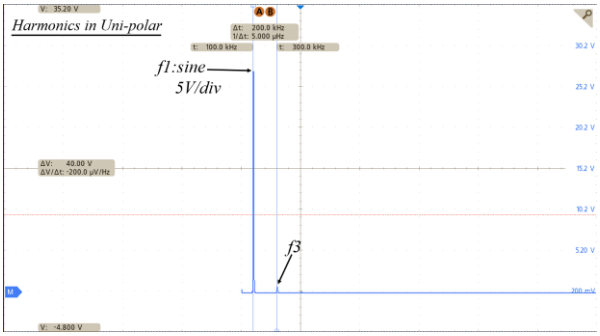


Fig. 7. Experimental BD switching waveform of the full-bridge midpoint (red) and output sine (blue)

As a result of driving circuit with both methods, the effect of harmonics is remarkable on sine waveform. In Fig. 8 shown amplitude voltage spectrum. It was seen that bipolar switching was clearly ahead in term of harmonic contents. Especially second harmonic. On the other hand, unipolar result has lower harmonics in the high-freq. Class-D amplifier output stage. In addition to these observations, 93% efficiency was measured.



(a)



(b)

Fig. 8. FFT comparison of output sines generated with *(a)* AD and *(b)* BD PWM

5. Discussion and Future Works

Although the use of GaN FETs may seem overly complex, we believe that our paper will serve as a practical user guideline for researchers and design engineers who seeks to utilize GaN Power ICs not only for Class-D but also for other high frequency power electronics applications. The high frequency class D amplifier is used in various equipment such as industrial flaw detection, piezoelectric drivers, test equipment, ultrasound medical imaging etc. The THD value of output signal can be reduced by increasing the switching frequency above one MHz. If switching frequency is increased, the fundamental frequency can be raised easily. In this way, it can also be used in different types of equipment.

6. Conclusions

In this research study, we presented a design guide and practical implementation of a high frequency Class-D power amplifier by utilizing Half-Bridge configurated GaN FET Power ICs and STM32 microcontroller. These ICs that have fast protection circuits and reduce dV/dt and dI/dt make driving of gates significantly easier. The prototype, which has 93% efficiency and 40W power with 2.15% THD provides practical information on both hardware and software by demonstrating that it achieves lower THD in unipolar switching on the Class-D.

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