A High-Precision Bandgap Reference with −0.063 ppm/°C Temperature Coefficient in a 45 nm CMOS Process

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Abstract

This study presents the design, device characterization, and simulation of a Bandgap Reference (BGR) circuit using 45nm CMOS technology. Three vertical pnp transistors with varying silicon areas were characterized to select an optimal device for CTAT generation. The PTAT generator's resistor ratios were optimized over a –40 °C to 125 °C temperature range to achieve first-order cancellation. A schematic-level BGR was developed by combining both CTAT and PTAT, incorporating a startup circuit to prevent the BGR from settling into a zero-current state. The final design achieves an output voltage of approximately 1.63 V with an exceptional temperature coefficient of −0.063 ppm/°C. The primary contribution of this work is achieving ultra-high thermal stability without the use of explicit, complex curvature-compensation circuitry, relying instead on the inherent cancellation of second-order effects through systematic device selection. This represents a deliberate trade-off, prioritizing exceptional thermal stability over low-voltage compatibility and area efficiency.

1. Introduction

A bandgap reference (BGR) circuit is a type of circuit that provides a constant voltage close to the bandgap of silicon (1.12 V) across temperature and process variations, which is essential for high-performance analog blocks such as ADCs, DACs, and voltage regulators. Temperature dependence is significant because even minor thermal shifts can degrade performance, resulting in gain reduction, signal distortion, and accuracy errors. Achieving this temperature independence also tends to bring about process independence, ensuring uniform performance despite variations in chip-to-chip manufacturing [1]. Designers often opt for CMOS over traditional BiCMOS processes for cost. While CMOS lacks native BJTs, the exponential I-V characteristics of bipolar transistors are ideal for generating the required positive and negative temperature coefficients. Therefore, a common design strategy is to exploit the inherent parasitic vertical pnp bipolar transistors that are formed within the standard CMOS substrate [1, 3, 4]. While many BGRs use complex curvature-compensation (CC) circuits, the primary contribution of this work is the demonstration of an ultra-low temperature coefficient (TC) of −0.063 ppm/°C in 45 nm CMOS using a first-order topology. This exceptional stability is achieved through the inherent cancellation of second-order effects, a result of systematic device characterization and high-gain scaling.

All circuits in this work are designed and simulated using the Cadence Virtuoso design environment and the Spectre simulator. The design utilized a generic 45 nm CMOS Process Design Kit (PDK), which provided industry-standard BSIM4 models for all MOS transistors and models for the parasitic vertical pnp transistors. Temperature sweeps are conducted from –40 °C to 125 °C. The models for the polysilicon resistors (R_1 and R_2) included their inherent Temperature Coefficient of Resistance (TCR).

The remainder of this paper is organized as follows. Chapter 2 details the design of the CTAT voltage generator. Chapter 3 presents the complementary PTAT voltage source. The complete BGR core, which combines these two blocks, is described in Chapter 4. Chapter 5 explains the necessity and implementation of the startup circuit. Finally, Chapter 6 concludes the paper.

2. CTAT Generation

A Complementary-To-Absolute-Temperature (CTAT) voltage is generated using the base–emitter voltage (V_{be}) of vertical pnp transistors available in the 45 nm CMOS with a temperature coefficient (TC) of approximately −2 mV/°C. A CTAT voltage or current decreases as absolute temperature rises.

$$V_{be} = \frac{KT}{q} ln\left(\frac{I_C}{I_S}\right) \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, and q is the elementary charge. The term I_C is the collector, and I_S is the temperature-dependent saturation currents.

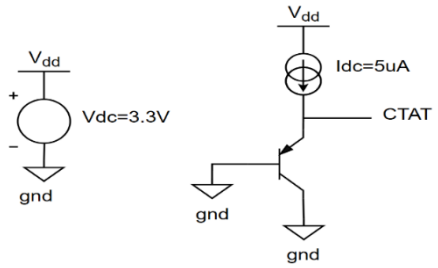

Figure 1: Schematic of the CTAT generator

As shown in Figure 1, the CTAT voltage is derived directly from the base-emitter junction, with a supply voltage of 3.3 V and a bias current of 5 µA. The same schematic is simulated three times, keeping all external parameters (including the bias current and output voltage) unchanged, replacing the pnp device with three variants of different sizes, corresponding to emitter areas of 2, 5, and 10 times that of a unit device (vpnp2, vpnp5, and vpnp10, respectively).

2.1. Device characterization

Based on the characterization data in Table 1, the vpnp5 device was selected as the optimal candidate for the CTAT generator. Its mid-value TC of −1.95 mV/°C is closest to the ideal silicon diode slope of −2 mV/°C, as shown in Figure 3.

The other variants were rejected. As summarized in Table 1, the vpnp10's TC (−2.19 mV/°C) was too high, which would lead

result in overcompensating the PTAT voltage in the final BGR. The vpnp2's TC of −1.63 mV/°C, was too shallow, which would lead to undercompensation. Therefore, vpnp5 is the most appropriate choice for a predictable and stable BGR design.

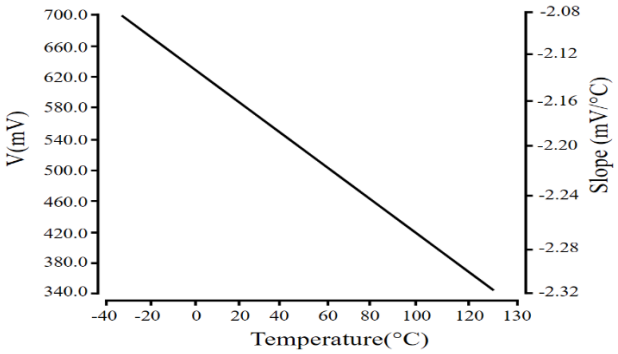

Figure 2: Simulated V_{be} versus T for the vpnp10 device variant.

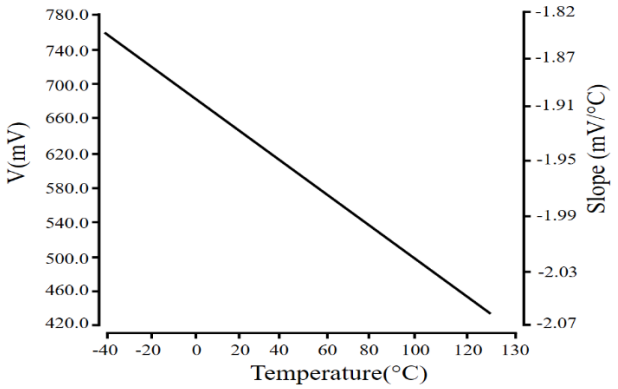

Figure 3: Simulated V_{be} versus T for the vpnp5 device variant.

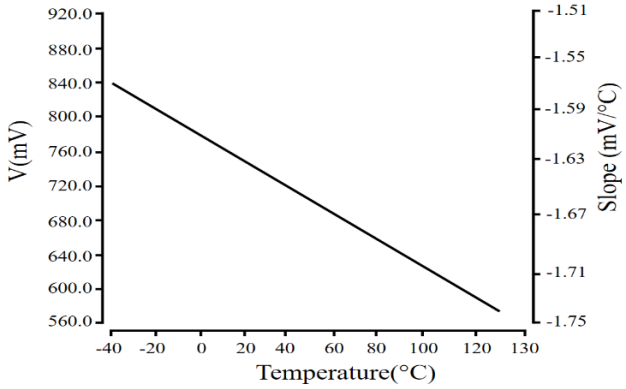

Figure 4: Simulated V_{be} versus T for the vpnp2 device variant.

Table 1. Comparison of Simulated CTAT Slope Ranges for Vertical PNP Transistors

PNP Device	CTAT Slope Range (mV/°C)	Mid-value (mV/°C)
vpnp10	-2.06 to-2.32	-2.19
vpnp5	-1.82 to-2.07	-1.95
vpnp2	-1.51 to-1.75	-1.63

Apart from the significant thermal coefficient, other factors, such as, silicon area and device matching, were also considered, further solidifying the choice of vpnp5. These variants (vpnp2, vpnp5, vpnp10) actually refer to the number of unit transistors being used; this directly impacts the physical footprint. Even though vpnp2 would yield the most area-efficient layout, it is highly susceptible to process-induced mismatch due to its small size. On the other hand, vpnp10 being the biggest device would provide better matching characteristics; however, it would still require a much bigger silicon area. The vpnp5 variant is considered the best compromise that allows a moderate outline to be made while achieving significantly higher matching performance and thus enabling a design that is not only area-conscious but also resistant to random process variations [5].

3. PTAT Generation

The Proportional-To-Absolute-Temperature (PTAT) voltage is obtained from the difference in base–emitter voltages ΔV_{be} between two vpnp5 devices operating at different current densities. This circuit is designed to produce an output voltage that increases linearly with absolute temperature.

$$\Delta V_{be} = \frac{KT}{q} \ln(n) \tag{2}$$

In this design, two identical vpnp5 devices are used, with one biased at a current density n = 2 times higher than the other. Thus, the theoretical PTAT slope is calculated by differentiating Eq. (1) with respect to temperature:

$$\frac{d(\Delta V_{be})}{dT} = \frac{k}{q}\ln(2) \approx 0.0597\, mV/°C \tag{3}$$

This calculated positive slope is designed to cancel the negative slope of the CTAT voltage by scaling through resistor ratios.

As shown in the schematic in Fig. 5, the PTAT voltage generator circuit is implemented with a 3.3 V supply and a bias current of 5 µA, which is mirrored in another branch of the PTAT. Both resistors R_1 and R_2 have values of 3.6 kΩ, which are tuned later to cancel the slope of CTAT. The circuit is simulated over the range −40 °C to 125 °C. The simulation results, plotted in Fig. 6, verify the circuit's functionality, showing a linear increase with temperature.

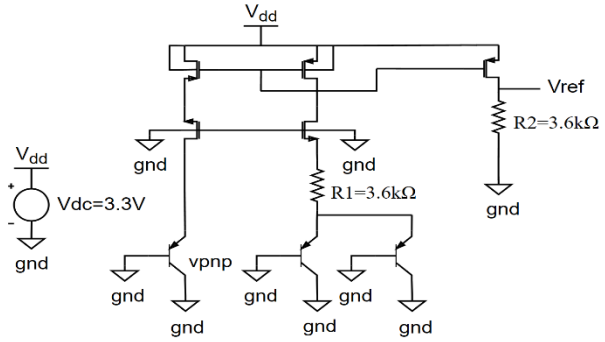

Figure 5: Schematic of the PTAT voltage generator

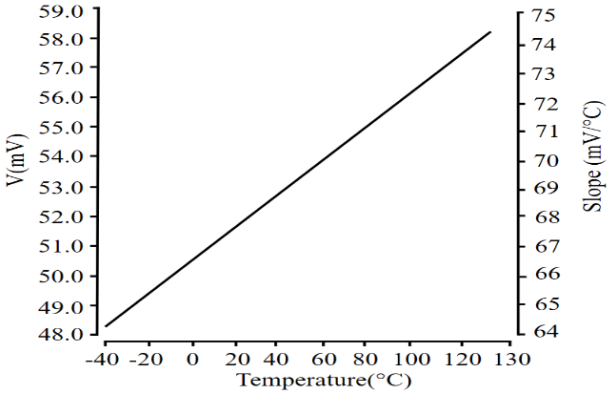

Figure 6: Simulation of the PTAT voltage generator

When the simulated performance is compared with the theoretical predictions, the differences between the two are slight. The temperature coefficient of the first order, which is the most ideal for this kind of circuit (if a BJT area ratio n = 2 is assumed), is roughly 59.7 µV/°C at room temperature. The simulation yielded a value of approximately 70 µV/°C at room temperature. Most of this difference is due to the non-idealities that are not accounted for in the first-order theory. The main reason is the absolute temperature coefficient of the physical resistors R_1 and R_2 that change the PTAT current as well as the voltage. Moreover, some second-order effects, like the temperature dependence of the BJT saturation current (I_s). Any thermal drift in the amplifier offset voltage is a factor that leads to a change in the slope and slight non-linearity (curvature) of the output plot [6].

4. BGR Core

The complete BGR is formed by summing a CTAT voltage and a PTAT voltage. But the absolute value of the positive TC from the PTAT voltage is much smaller than that from the CTAT voltage. Hence, just a pure one-to-one addition would still give a voltage with a negative overall TC. To achieve a total one-to-one cancellation, the PTAT voltage must be scaled by a specific constant k.

$$\Delta V_{ref} = CTAT + k.PTAT \quad (4)$$

The resistor ratio in the BGR core determines the value of k. For first-order compensation:

$$\frac{d(V_{ref})}{dT} \approx 0 \quad (5)$$

The calculated optimum value of k is physically realized in the circuit by setting the resistor ratio.

$$k = \frac{R_2}{R_1} \quad (6)$$

Based on the design, the values of the resistors are taken as: R_1 = 3.6 kΩ and R_2= 85.4 kΩ. With these component values, the scaling factor k is:

$$k = \frac{R_2}{R_1} = \frac{85.4}{3.6} \approx 23.72 \quad (7)$$

This first-order method minimizes the temperature drift but may still require higher-order curvature correction in deep submicron processes for very low ppm/°C performance.

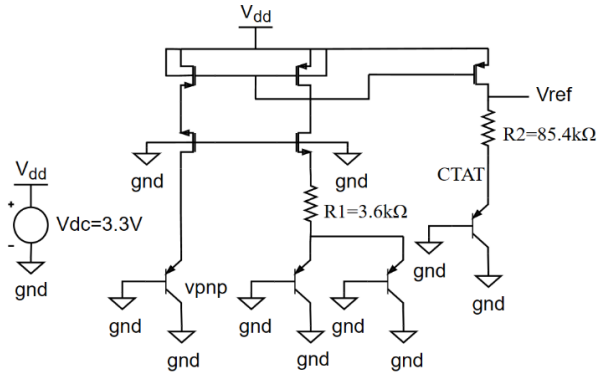

Figure 7: Complete schematic of the first-order BGR core.

The schematic, shown in Figure 7, illustrates the integrated design which operates from a 3.3 V supply. vpnp5 device is selected as the core bipolar transistor. The circuit is biased with a current of 5 µA, which is distributed and mirrored to the necessary branches. The PTAT voltage is generated across the resistor R_1(3.6 kΩ), while the scaling and summation are performed using the resistor R_2 (85.4 kΩ). This specific ratio of R_1 and to R_2 is chosen to ensure the negative TC of the CTAT component is canceled by the positive TC of the PTAT component. While this results in a stable reference voltage, it requires a significant scaling factor k, of approximately 23.72.

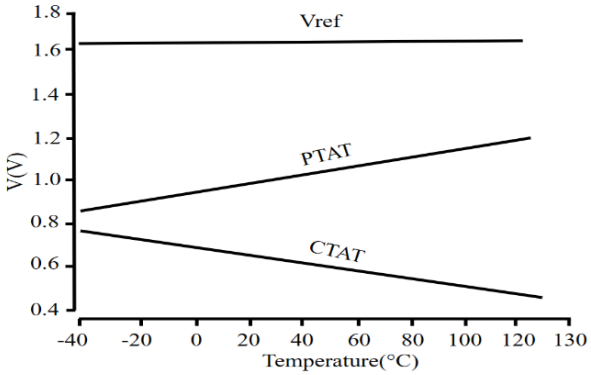

Figure 8: Simulated output reference voltage versus temperature for the complete BGR circuit.

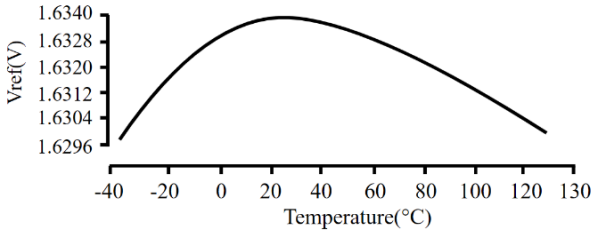

Figure 9: A zoomed-in plot of V_{ref} from Fig. 8, showing its characteristic curvature over the whole temperature range.

Figure 8 presents a graphical summary of the BGR circuit performance, effectively illustrating the successful implementation of first-order temperature compensation. This figure demonstrates how the central elements of the circuit interact over the

range of −40°C to 125°C. The line labeled CTAT shows a voltage with the characteristic negative TC, while the line labeled PTAT shows a voltage with the expected positive TC. The final output, labeled V_{ref} is the weighted sum of these two opposing voltages. As shown by its nearly flat profile, the linear temperature drifts have been almost completely canceled, resulting in a highly stable output voltage. The large linear drifts, as shown in Figure 8, are almost eliminated, resulting in a very stable output voltage of approximately 1.63 V. The zoomed-in view of V_{ref} discloses the typical residual curvature of a first-order design. The curve, which is, after all, a parabola, suggests that the linear TCs are compensated. At the same time, the non-linear, second-order effects still exist, which are ultimately responsible for the circuit's small temperature coefficient.

4.1. Temperature Coefficient Analysis

TC is the primary indicator of a voltage reference's quality, measuring its stability across various temperatures. This approach characterizes the stability by connecting the output voltage at the lowest temperature with that at the highest temperature by a straight line. The gradient of this line, which has been adjusted to the standard output voltage, shows the average linear change of the device with time [6].

The TC of a BGR is extracted by measuring the output voltage drift between the cold corner (−40°C) and the hot corner (125°C). The linear TC is calculated as:

$$TC = \frac{V_{ref}(125°C) - V_{ref}(-40°C)}{V_{nominal} \times \Delta T} \times 10^6 \text{ ppm/°C} \quad (8)$$

From the simulation results, the following values are obtained:

$$V_{ref}(-40°C) = 1.629743\,V$$
$$V_{ref}(125°C) = 1.629726\,V$$
$$V_{nominal} = 1.633906\,V\ (at\ 25.05679°C)$$
$$\Delta T = 165°C$$

Substituting these values into Eq. (8), we get:

$$\text{TC} = -0.063 \text{ ppm/°C} \quad (9)$$

While the final simulated TC of −0.063 ppm/ °C suggests extraordinary thermal stability, this result must be benchmarked against other recent publications to validate its performance.

Table 2. Comparison with State-of-the-Art BGR Circuits

Reference	Year	Technology (nm)	TC (ppm/°C)	V_{ref} (V)	Min V_{DD} (V)
[9]	2019	90	6.81	0.28	0.9
[10]	2020	65	1.08	0.49	1.2
[11]	2021	180	45	0.22	0.5
[12]	2025	N/A	0.855	≈1	1.2
This work	**2025**	**45**	**−0.063**	**1.63**	**1.8**

Table 2. offers a thorough comparison with a number of state-of-the-art (SOTA) BGR circuits that have been published recently in order to place the performance of this work within the current research context. As demonstrated, these SOTA designs include sub-1V (sub-1-Volt) circuits [9, 11] as well as other low-voltage topologies [10, 12], with minimum supply voltages ranging from 0.5 V to 1.2 V. Even the best-performing works achieve TCs in the high-precision range of 0.855 ppm/°C [12] to 6.81 ppm/°C [9]. The suggested design in 45 nm CMOS, on the other hand, achieves an exceptionally low temperature coefficient of −0.063 ppm/°C. This result is over 13.5 times more stable than the high-precision 2025 design [12] and over 17 times more stable than the 65 nm design [10].

As explained in Section 6, this ultra-high precision is the consequence of a conscious design trade-off. Due to the large scaling factor (k ≈ 23.72) needed for the first-order cancellation, it is accomplished at the known cost of a higher reference voltage (1.63 V) and a higher minimum supply voltage (1.8 V). This validates the goal of the paper, which is to present a design that puts high-performance systems' outstanding thermal stability ahead of other applications' low-voltage, area-efficient needs.

4.2. Power Supply Rejection Ratio (PSRR) Analysis

Further analysis was conducted to verify the circuit's stability. As shown in Figure 10, a Power Supply Rejection Ratio (PSRR) simulation demonstrates a DC rejection of −7.5 dB. This poor PSRR is expected for this simple, open-loop topology which does not include advanced cascoding, and its improvement is a clear objective for future work.

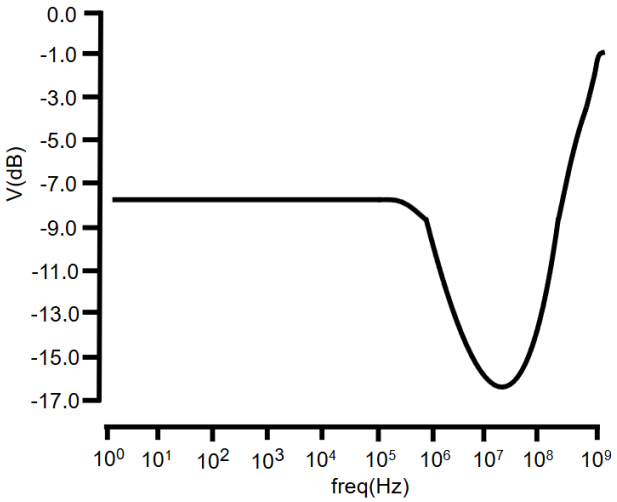

Figure 10: Simulated Power Supply Rejection Ratio (PSRR) vs. Frequency, showing a DC PSRR of -7.5 dB.

5. Startup circuit

A BGR exhibits two possible operating points. Normal state, where it works fine, and zero-Current state, where all branch currents are equal to zero, resulting in V_{ref} = 0 V. If the circuit goes into the zero-current state, it will remain stuck there forever. Therefore, there must be a mechanism to pull the BGR circuit from zero current state to normal state. This mechanism is implemented using a circuit called the startup circuit. It is very important that the start-up circuit completely disables itself and becomes totally invisible to the core when the BGR is on. It would alter the carefully balanced bias currents, which would degrade the circuit's precision and ruin its temperature coefficient optimization [8].

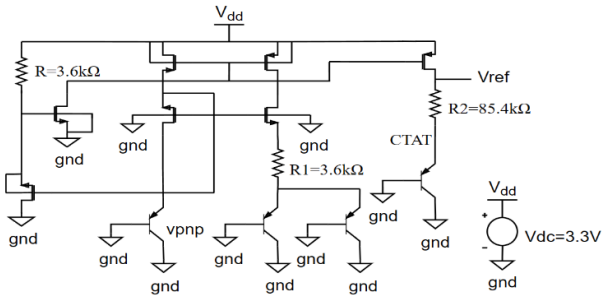

Figure 11: Startup schematic.

Figure 11 shows the complete schematic of the BGR, with the startup circuit. During power-on, if the BGR core settles in the zero-current state, the start up circuit activates and injects a small current into the core, forcing it into the correct operating state.

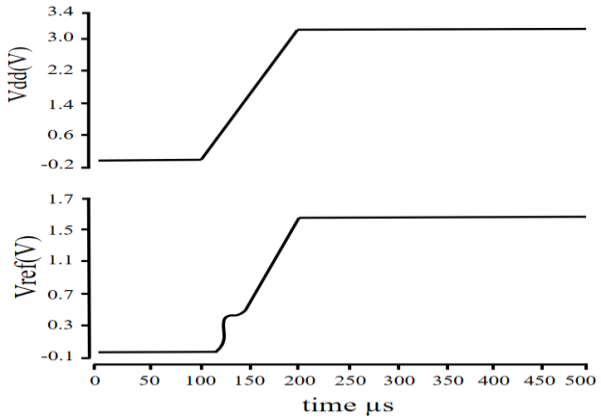

Figure 12: Startup simulation

Figure 12 presents the transient simulation results, which demonstrate a successful startup sequence for the reference voltage. Initially, the startup circuit detects the zero current state and injects a current into the BGR core, pulling it out of the undesired zero-current state. In the transient simulation, the supply voltage V_{DD} ramps from 0 V to 3.3 V starting at $t = 100$ µs and finishing at $t = 200$ µs. Correspondingly, the reference voltage (V_{ref}) initially remains at 0 V but begins to rise once the supply crosses the threshold, eventually settling at ≈1.6 V by 200 µs. Once the BGR enters its normal working state, the startup circuit automatically deactivates itself and becomes transparent to the core. This demonstrates a robust startup time of approximately 100 µs.

6. Conclusions

This paper presented a 45 nm CMOS BGR design achieving an exceptional TC of −0.063 ppm/°C**.** This high thermal stability, however, comes at the cost of a high reference voltage (1.63 V) and a large 85.4 kΩ resistor. This high (V_{ref}) makes the circuit incompatible with low-voltage systems, pushing the minimum required supply to 1.8 V or more. The large resistor sacrifices area efficiency and contributes significant thermal noise. In the end, this design is not intended for low-power applications, but tailored for specialized, high-performance systems where its exceptional thermal stability is the critical requirement and these trade-offs are acceptable. For future work, several improvements will be investigated to address these limitations. A critical next step is a thorough analysis of the circuit's output noise performance, which was not completed for this study. Subsequent work will also focus on improving the poor − 7.5 dB PSRR through techniques such as cascoding, as well as low-voltage adaptation by exploring current-mode topologies to reduce V_{ref}. Additionally, digital trimming techniques will be incorporated to compensate for process variations. Finally, the design a strong candidate for migration to a foundry-specific PDK for silicon validation (tape-out), which would be required to measure its real-world performance against these promising simulation results.

7. Acknowledgments

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8. References

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