NEW MEMRISTOR EMULATOR CIRCUIT USING OTAs AND CCIIs

Hasan Sözen[1], Uğur Çam[2]

[1]Celal Bayar University, Department of Electrical and Electronics Engineering,
Muradiye Campus, Muradiye, 45140, Manisa, Turkey
hasan.sozen@cbu.edu.tr
[2]Dokuz Eylül University, Department of Electrical and Electronics Engineering,
Tınaztepe Campus, Buca, 35160, İzmir, Turkey
ugur.cam@deu.edu.tr

Abstract

In this paper, a new memristor emulator circuit is proposed. It is realized by operational transconductance amplifiers (OTAs) and second generation current conveyors (CCIIs). A mathematical model to describe the behavior of presented circuit is derived. Memristance value of the emulator circuit is adjustable by means of a simple change of transconductance parameter (g_m) of operational transconductance amplifier in the emulator circuit, amplitude and frequency value of applied voltage across terminals of memristor emulator. Frequency dependent pinched hysteresis loop in the current versus voltage plane holds up to 5 kHz. The breadboard experiment of proposed emulator circuit is built by using CA3080 and AD844 ICs for transconductance amplifier and second generation current conveyor respectively. The results of SPICE simulation and experimental test are given to verify the theoretical analyses. The presented emulator circuit can be used in real world memristor circuit applications such as chaotic systems, programmable analog circuits.

1. Introduction

Memristor, the fourth fundamental two terminal circuit element, was postulated in 1971 by Prof. Leon Chua. It defines the missing relation between flux and charge and behaves as a nonlinear resistor with memory [1]. Memristor concept was generalized to much broader class called memristive systems by Chua and Kang in 1976 [2]. Both memristor and memristive devices have the pinched hysteresis loop in the current versus voltage plane. Thus, the resistance of the device depends on the time history of the current flowing through it. Under sinusoidal excitation the area of the pinched hysteresis loop is inversely proportional to frequency of voltage signal across the memristor [2]. On May 1, 2008 Stanley Williams and his group realized memristor in device form using two-terminal titanium dioxide (TiO_2) nanoscale device [3]. Recently the notion of memristive systems were extended to memcapacitive and meminductive systems and the special cases of the newly extended systems were defined as memcapacitors and meminductors [4].

It is important to have a simulation model of memristive devices to investigate their effects in electronic circuits. In the literature numerous SPICE models for memristor [5-16], memcapacitor [17] and meminductor [18] have been presented to give possibility to designers verifying their theoretical analyses. Currently, a commercial memristor, memcapacitor and meminductor devices are still not available for experimental research. To develop a real memristive device, emulator circuits have been proposed for breadboard experiments. Emulator circuits of memristor [19, 28], have been proposed to give possibility applying memristor practically in electronic circuits. In [19] an emulator of memristor using digital potentiometer, microcontroller and analog to digital converter was proposed and used in programmable analog circuits. It has some drawbacks due to resolution of digital signal and digital potentiometer. Some of memristor emulators have grounded restriction [20, 21]. A memristor emulator was designed and used to obtain memcapacitor emulator by Yu et al. [22]. In [23, 24] flux controlled memristor emulator circuit using current conveyors was presented. A floating memristor emulator circuit was designed and used in a circuit to obtain meminductive circuit [25]. Yesil et al. designed memristor emulator circuit using DDCC based on CMOS [26]. In [27] two memristor emulator circuits, voltage controlled and current controlled, was presented which behaves as the proposed model given in same study. Memristor emulator circuit consists of OTA and current feedback operational amplifier was presented and used in a multivibrator circuit [28]. In [29-32] emulator circuits for memcapacitor and meminductor devices were presented.

In this paper, we present a novel memristor emulator by making use of operational transconductance amplifiers and second generation current conveyors and built it using ICs of used devices. The rest of the paper is organized as follows. In Section 2 we introduce a flux controlled memristor emulator circuit. Simulation results and experimental test measurements which belong to presented circuit are given in Section 3, followed by conclusion in Section 4.

2. Flux Controlled Memristor Emulator Circuit

Memristor is the fourth fundamental circuit element owing to its characteristics cannot be duplicated by any combination of other fundamental circuit elements. It defines the nonlinear relationship between charge q and flux φ. For a charge controlled memristor its relation is $\varphi(t) = \varphi(q)$, if the memristor is flux controlled its relation becomes $q(t) = q(\varphi)$. For a flux controlled memristor nonlinear constitutive relationship between the memristor terminal voltage v and the internal current i can be written as following equation.

$$v(t) = M(\varphi)i(t) \tag{1}$$

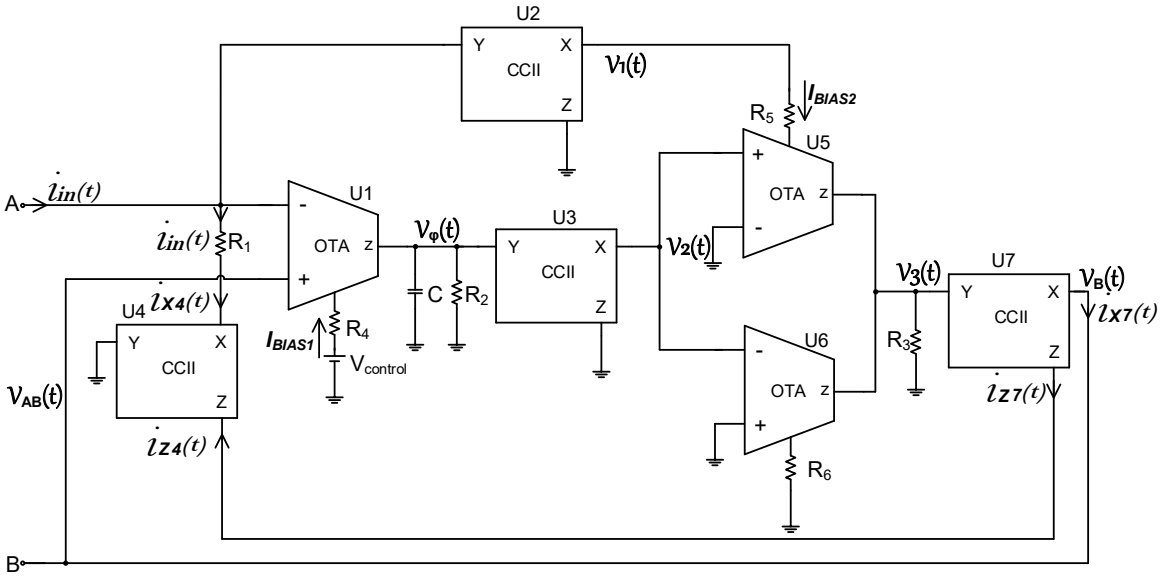

Fig. 1. Emulator circuit for memristor

In this paper, the proposed circuit emulates a flux controlled memristor element. It consists of three operational transconductance amplifiers, four second generation current conveyors, six resistors and one capacitor elements as given in Fig. 1. The g_m parameter of OTA is proportional to the current flowing through its bias current terminal. The g_m parameters of U5 and U6 are used for multiplication process. Therefore only g_m parameter of U1 (g_{m1}) can be used to change memristance value besides frequency and amplitude of input voltage.

In ideal case, current flowing through input terminals of operational transconductance amplifier and terminal Y of CCII is zero. Hence for the presented circuit all current passes through the resistor R_1. Input current can be written as following by defining $v_A(t)$ as voltage at node *A*.

$$i_{in}(t) = \frac{v_A(t)}{R_1} \tag{2}$$

From Faraday's Law, in order to obtain flux crossing across terminals *A* and *B* the integral of $v_{AB}(t)$ have to be obtained. U1 with capacitor C (omitting R_2) perform integral function. R_2 is used to eliminate the output offset of the integrator U1-C. The mathematical relation of integrator in case of ignoring DC level can be written as;

$$v_\varphi(t) = -\frac{g_{m1}}{C}\int (v_A(\tau) - v_B(\tau))d\tau \tag{3}$$

Since the flux is defined as $\varphi(t) = \int (v_A(\tau) - v_B(\tau))d\tau$, (3) can be written as $v_\varphi(t) = -\frac{g_{m1}}{C}\varphi(t)$.

U2 and U3 are used to copy voltages $v_A(t)$ and $v_\varphi(t)$ without any current copying to their terminal X, since the current flowing through terminal Y of CCII is zero [32]. U4 is used together with U7 to perform the input current to flow through node *B* since the current flowing through terminal X of CCII is equal to current flowing through terminal Z. Thus the following relations are obtained.

$$i_{in}(t) = i_{X4}(t) = i_{Z4}(t) = i_{Z5}(t) = i_{X5}(t) = i_B(t) \tag{4}$$

OTA pairs U5 and U6, with equal resistors connected to their bias terminals, R_5=R_6, are used to multiply the voltages $v_1(t)$ and $v_2(t)$ denoted in Fig. 1 [34]. The mathematical description of multiplying process can be obtained as;

$$v_3(t) = -\frac{g_{m1}\varphi_{AB}(t)v_A(t)R_3}{2V_T R_5 C} \tag{5}$$

where V_T is the thermal voltage given by KT/q. Besides performing the input current to flow through node *B*, U7 is used to copy the voltage $v_3(t)$ to node *B* and provides all current at outputs of U5 and U6 to flow through R_3 resistor. Hence, the voltage across the emulator circuit can be written as;

$$v_A(t) - v_B(t) = i_{in}(t)R_1 + \frac{g_{m1}\varphi_{AB}(t)v_A(t)R_3}{2V_T R_5 C} \tag{6}$$

Current voltage relation of memristor is obtained as in (7) by substituting (2) in (6). It is obvious from (7) that the memristance expression for flux controlled memristor emulator circuit can be obtained as given in (8).

$$v_{AB}(t) = i_{in}(t)\left[R_1 + \frac{g_{m1}R_1R_3\varphi_{AB}(t)}{2V_T R_5 C}\right] \tag{7}$$

$$M_{AB}(\varphi) = \left[R_1 + \frac{g_{m1}R_1R_3\varphi_{AB}(t)}{2V_T R_5 C}\right] \tag{8}$$

It is clear from (8) that memristance consists of connected series a linear time invariant resistor with a time varying resistor depends on flux and g_{m1}. Assuming that the power supply for

used ICs is ±V_{dd} and a sinusoidal voltage $v_{AB}(t)=v_m sin(2\pi ft)$ is imposed on terminals A and B and ignoring DC level at output of integrator, the memristance can be calculated as;

$$M_{AB}(\varphi)=\left[R_1-\frac{g_{m1}R_1R_3v_m\cos(2\pi ft)}{4\pi fV_TR_5C}\right] \quad (9)$$

In order to obtain positive memductance value the frequency of input voltage must satisfy the following condition;

$$f>\frac{g_{m1}R_3v_m}{4\pi V_TR_5C} \quad (10)$$

Therefore, based on (9) and (10), and the configuration of $v_A(t)$- $v_B(t)$, all the possible values of memristance satisfy;

$$0<M_{AB}<2R_1 \quad (11)$$

The relationship between time variant and time invariant parts of memristance denotes the frequency and g_{m1} dependence of pinched hysteresis loop. The relationship between two parts can be described by the ratio of their amplitudes as following.

$$k=\frac{g_{m1}R_3v_m}{4\pi fV_TR_5C} \quad (12)$$

Since voltages on circuit branches must be bounded by power supply voltage V_{dd}, it is logical using f and g_{m1} as control parameters of pinched hysteresis loop rather than v_m. It is obvious from (12) that increasing f will decrease k on the contrary g_{m1} and vice versa. Therefore, g_{m1} and f can be used for holding pinched hysteresis loop at high frequencies. When $k\to 0$, the memristance approximates to linear resistor, whereas $k\to 1$ the memristance has the maximum pinched hysteresis loop. If $k\geq 1$ the memristance value will have negative or zero value due to "$cos(2\pi ft)$" expression in (9).

3. Simulation Results and Experimental Tests

The proposed memristor emulator circuit is simulated using PSPICE simulation program to verify theoretical analyses. SPICE models of CA3080 and AD844 ICs are used for OTA and CCII devices respectively to achieve the simulation results. The circuit parameters given in Table 2 are used in simulations to operate the emulator circuit for different frequency ranges. Comparison of presented memristor emulator circuit with others published in literature is given in Table 1.Values of R_2 and C are changed as given in Table 2 to provide memristor hysteresis holds up 5 kHz.

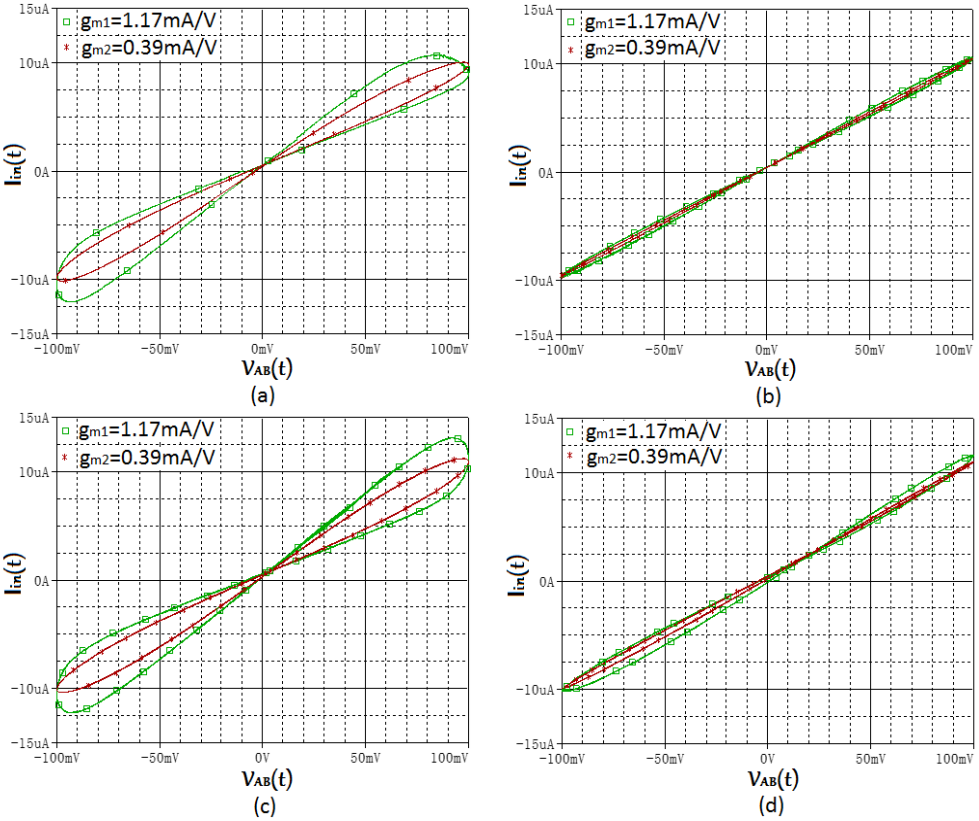

Fig. 2. Frequency dependent pinched hysteresis loop of memristor emulator circuit for different frequencies: a) 10 Hz, b) 100 Hz, c)1 kHz, d) 5 kHz

Table 1. Comparison of presented emulator circuit with others published in literature.

Emulator	Maximum frequency for memristor regime	Control parameter of emulator
[19]	50 Hz	V_m
[20]	800 Hz	V_m, f_m
[21]	2 Hz	V_m, f_m
[22]	50 Hz	V_m, f_m
[23]	20.2 kHz	V_m, f_m
[24]	120 Hz	V_m, f_m
[25]	16 Hz	V_m, f_m
[26]	1 MHz	V_m, f_m
[27]	100 Hz	V_m, f_m
[28]	600 Hz	V_m, f_m
Presented	5 kHz	V_m, f_m g_m

Table 2. Component List used in emulator circuit

Element	Value	Frequency Range
V_{dd}-CA3080	±15V	
V_{dd}-AD844AN	±5	
V_m	100mV	
R_1	10 KΩ	
R_3	15 KΩ	
R_4	500 KΩ	
R_5	200 KΩ	
R_6	200 KΩ	
C	100 uF-R_2=5 KΩ	1 Hz-10 Hz
	10 uF-R_2=10 KΩ	10 Hz-100 Hz
	1 uF-R_2=20 KΩ	100 Hz-1 kHz
	100 nF-R_2=40 KΩ	1 kHz-5 kHz

Simulation results given in Fig. 2 are obtained for two distinct frequency ranges, 10 Hz-100 Hz and 1 kHz - 5 kHz. Fig. 2 (a) and (b) show the simulation results for 10 Hz-100 Hz frequency range while Fig. 2 (c) and (d) gives the results for 1 kHz - 5 kHz frequency range for each g_{m1} parameters, 1.17 mA/V and 0.39 mA/V. It is obtained from simulation results that the reaction of pinched hysteresis loop is different for each frequency range due to value of capacitor C in the integrator block which confirms (8) and (9). While the value of C is choose high, the variation of memristance becomes smaller and vice versa. Fig. 2 (a) is obtained at 10 Hz frequency value of input voltage whereas Fig. 2 (b) gives the simulation results at 100 Hz. Memristance characteristic in Fig. 2 (b) turns into linear resistor at 100 Hz while in Fig. 2 (c) it has hysteresis loop at 1 kHz frequency due to the values of passive elements given in Table 2. The pinched hysteresis loop leads to linear resistor at 5 kHz for g_{m1} equals to 0.39 mA/V as given in Fig. 2 (d). As it is appeared from the simulation results given in Fig. 2 (a)-(d) frequency dependence of hysteresis loop can be controlled via g_{m1} parameter and largely of C and R_2 elements. Therefore it becomes possible to holding up memristance characteristic at high frequencies.

The breadboard experiment of proposed emulator circuit is built using commercially available ICs CA3080 and AD844 for OTA and CCII elements respectively. Numerical values of passive elements are chosen as given in Table 2. It is aimed to confirm the correctness of the proposed emulator circuit together with SPICE simulation results. In order to obtain the

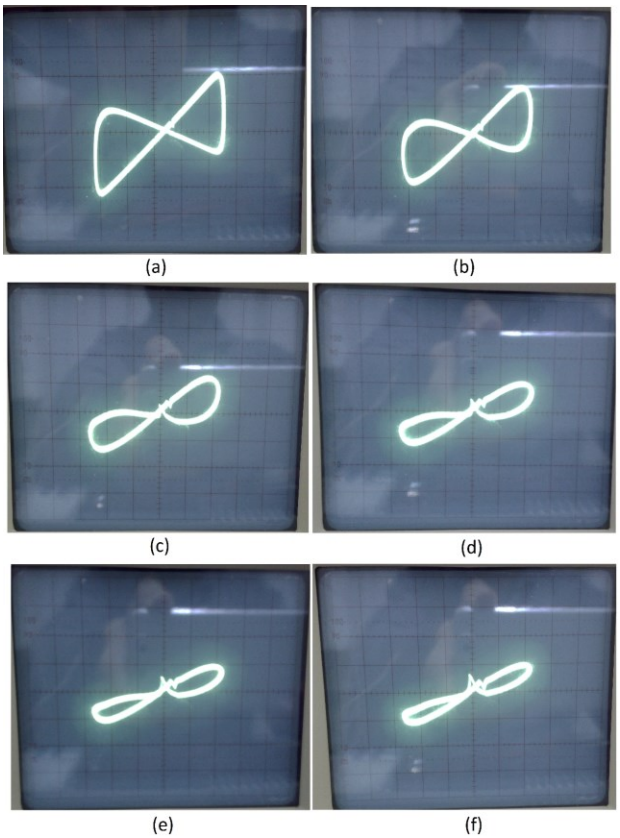

Fig. 3. Oscilloscope trace of the frequency dependent pinched hysteresis loop of memristor emulator circuit for different frequencies: a) 500 Hz, b)1 kHz c) 2 kHz, d) 3 kHz, e) 4 kHz, f) 5 kHz.

measurements from the experimental circuit, the signals are captured by oscilloscope NS 2040. Fig. 3 shows the measured oscilloscope display of the breadboard experiment circuit at 500 Hz, 1, 2, 3, 4 and 5 kHz frequencies for the values of C and R_2 equal to 100 nF and 40 kΩ. The pinched hysteresis loop is obtained measuring $v_A(t)$ versus $v_{AB}(t)$ since $v_A(t)$ is R_1 time of input current. Frequency dependence of the pinched hysteresis loop shows high accuracy with simulation results and mathematical model of memristor emulator circuit.

4. Conclusion

In this paper, a new emulator circuit of a flux-controlled memristor which composes of OTAs and CCIIS has been presented. The most significant feature of the proposed emulator circuit is the possibility of controlling memristance value by change of transconductance parameters of the used operational transconductance amplifiers via a bias voltage. By this way in addition to frequency and amplitude values of input voltage across memristor, transconductance parameter is added as a control parameter for memristance variation. The presented emulator circuit differs from other emulator circuits in the literature with this feature. The mathematical expressions are given to describe the behavior of presented circuit. CA3080 and AD844 ICs are used to build the emulator circuit for practical application of memristor. The oscilloscope measurements from the breadboard experiment circuit and SPICE simulation results verifies the theoretical analyses.

5. References

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