An 8Gb/s Serial Link Transceiver, using MPPM and PAM schemes

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Abstract

In this paper, a new efficient modulation technique, with 8-bit per symbol data rate is introduced to increase the data rate and decrease the power dissipation. Moreover, a new transceiver architecture is designed to implement the above modulation. The proposed modulation which is named MPPAM is developed by combining the advantages of MPPM modulation and PAM modulation. The return-to-zero nature of this modulation method has this potential to transmit the clock pulses and data together. It means the pin count is reduced by merging the clock signal and 8-bit data into a single transmitted channel. In addition, the need for the clock recovery circuit is mitigated. In the proposed modulation, the value of minimum pulse width (PW) is significantly larger than conventional non-return to zero data PW (Tb). Therefore, the value of ISI in the channel improves considerably.

1. Introduction

Nowadays, high-speed connections and links grow continuously. Providing a higher bandwidth for various systems such as computers, routers and chip-to-chip communications is an essential issue. Increasing the value of data transferring speed and reducing the value of power dissipation are two important factors in designing of serial link transceivers. The chip area and pin count will be increased by increasing the bus bandwidth. Therefore, the modulation techniques for transferring several bits over each symbol time, including multi-level signaling, have been proposed.

Further, transceivers based on multi-pulse amplitude modulation (M-PAM) are widely used nowadays. By using the PAM modulation, the data rate is increased significantly in comparison to the symbol rate [1][2]. However, PAM modulation technique has a character of non-return to zero format. Therefore, a complicated clock recovery system must be utilized to recover the clock from the incoming data.

To overcome the above problem, PWM modulation [3] is proposed in articles to combine with PAM [4][5][6]. The PWM modulation benefits from the advantages of RZ data structure. Therefore, the clock signal can easily be extracted at the receiver side. In [7], the optimum values of PAM voltage level and PWM pulse width levels were chosen to obtain the best values of data rate and also minimum pulse width. However, since the PWM structure had a low data rate property per symbol, the data rate was not high enough.

In this paper, a new modulation method is proposed, which is a combination of PAM and MPPM modulation and is called multi-pulse position amplitude modulation (MPPAM). By using the PPM modulation, the clock signal is embedded in the modulated data. It means that this modulation has an RZ data structure and the clock signal can easily be extracted from the modulated data. In addition, the MPPM modulation format can increase the data rate in comparison to symbol rate. Therefore, the combination of MPPM and PAM formats can increase the data rate considerably. In the proposed transceiver, 8 bits are transferred over 5-time slots per symbol. Therefore, the highest possible values of the minimum pulse width and also bit rate are achieved.

This paper is organized as follows: the concept of the proposed MPPAM is reviewed in Section 2. Sections 3 and 4 describe the architecture of transmitter and receiver, respectively. Conclusions are discussed in Section 5.

2. Proposed MPPAM modulation

2.1 MPPAM modulation structure

The proposed modulation is a combination of multi-pulse position modulation (MPPM) and pulse amplitude modulation (PAM), which is called multi-pulse position amplitude modulation (MPPAM) by the authors.

In the MPPAM-encoded signal, there are N+1-time slots per symbol. The first N time slots carry data bits and the last time slot is always equal to zero in differential mode output. The last time slot will help the PLL detect the start point of the transmitted symbol string at the receiver block. It means when the PLL detects a special situation of output values at the last time slot, which is not repeated at other time slots, PLL can be synchronous itself with the modulation structure. Accordingly, the proposed modulation is a kind of RZ structure.

Signaling scheme of the proposed MPPAM modulation format, in the presence of 5-time slots (N=4), is indicated in Fig.1 (a). The values of 4 even bits (0, 2, 4, 6) are resolved by MPPM modulation using the sign of waveform amplitude and the other 4 odd bits (1, 3, 5, 7) are determined by PAM modulation using the absolute value of waveform amplitude. The clock signal is also embedded at the last time slot. For example, at the first time slot, the values of the 0th and 1th bits are obtained as follows:

If WA > 0 then Bit0 = 1 else Bit0 = 0
& If | WA | > VR1 then Bit1 = 1 else Bit1 = 0, (1)

where WA indicates the value of waveform amplitude at the proportional time slot and VR1 is a reference voltage between two voltage levels. In the same way, at the transmitter side, the waveform is constructed using the following equation:

$$\textit{At the first time slot: Vout} = \begin{cases} V_R + \text{Bit0}\, V_R & \text{if} \quad \text{Bit1} = \text{'1'} \\ -V_R - \text{Bit0}\, V_R & \text{if} \quad \text{Bit1} = \text{'0'} \end{cases} \tag{2}$$

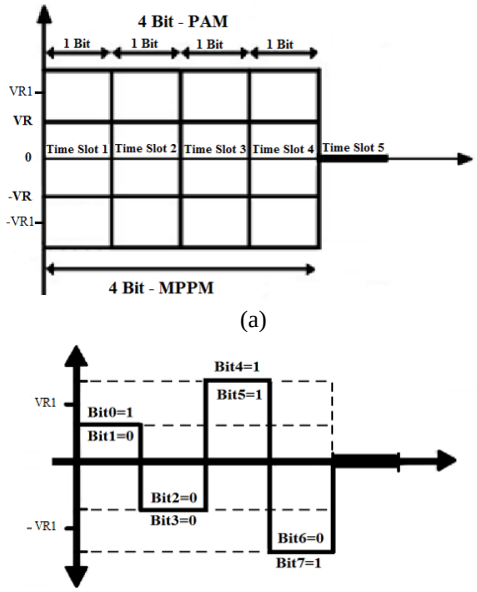


Fig. 1. (a) Signaling scheme of proposed MPPAM (b) An example of the proposed modulation waveform.

An example of the proposed modulation waveform is indicated in Fig.1b. The waveform is positive at time slots 1 and 3. As a result, the values of Bit0 and Bit4 are equal to '1'. This waveform is negative at time slots 2 and 4. Consequently, the values of Bit2 and Bit6 are equal to '0'. On the other hand, the absolute value of waveform is greater than V_{R1} (a reference voltage between VR and 2VR) at time slots 3 and 4. It means that the values of Bit5 and Bit7 are '1'. In the same way, the absolute values of waveform are less than V_{R1}, at time slots 1 and 2. Therefore, the values of Bit1 and Bit3 are '0'.

By combining an M-level PAM at N+1-time slots, the number of $Log_2^{M/2}$ bits per time slot (except for the final slot) is specified. Therefore, the value of bit rate per symbol is as follows:

$$MPPAM \quad Modulation \quad Bit\ Rate = N + N\ Log_2^{M/2} \qquad (3)$$

As a result, the proposed modulation causes a considerable increase in bit rate while the symbol rate remains constant. Increasing M and N will increase the value of bit rate more considerably. The value of ISI in the channel and also the maximum required on chip clock frequency are reduced due to the reduction of symbol rate in comparison to bit rate. To transmit the digital data toward the receiver, a limited bandwidth channel is used. Therefore, the values of amplitude and pulse width of the received signal will be reduced. Noticeably, extending the value of pulse width of transmitted data will improve the ISI in the channel. In the proposed MPPAM modulation format, in addition to increasing the value of bit rate, the value of minimum pulse width increases. The value of minimum pulse width in the proposed MPPAM method is defined as follows.

$$MPPAM \quad Minimum \quad PW = \frac{T_b\left(N + N\ Log_2^{M/2}\right)}{N+1} \qquad (4)$$

Increasing the values of M and N will increase the values of bit rate and minimum pulse width. However, increasing the value of M causes a decrease in level spacing of the signal and, therefore, an increase in the value of ISI in the channel. On the other hand, by increasing the value of N or the number of time slots, the complexity of the circuit will increase considerably. According to the above discussion, both M and N are considered equal to 4.

2.2 Transceiver architecture

The proposed 8-bit transceiver is shown in Fig.2. The transmitter part contains PLL block, slot selector and MPPAM modulator driver. In the PLL block, 10 clock phases are generated per 36º phase difference. These clock phases are used to create proper time slots at the next block. The final 8-bit MPPAM modulated output waveform is produced at MPPAM modulator block.

At the receiver side, there are three main building blocks, which include pre-amplifier circuit, PLL block and MPPAM demodulator block.

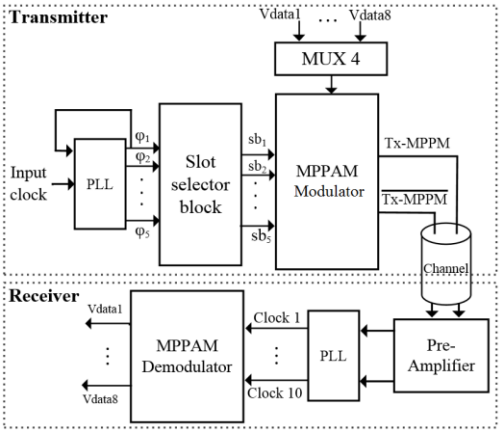


Fig 2. Proposed Transceiver Architecture.

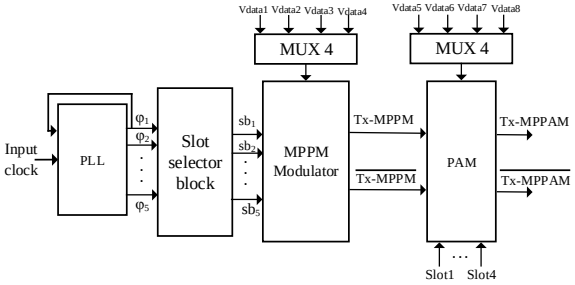


Fig 3. Proposed transmitter architecture.

3. 8-bit per symbol MPPAM transmitter

As shown in Fig. 3, Transmitter block contains PLL, slot selector block, MPPM modulator, 4×4 MUX and 4-PAM driver.

At the transmitter side, slot selector block provides 5 individual signals that are set to the high value at different 5 time slots. At each time slot, the proper value of output MPPM signal is produced according to the input even bits (Bits 0, 2, 4, 6). At the proportional time slot, if the value of input bit is 1, the output waveform will be set to the value of Vdd. Otherwise, it will be equal to –Vdd. The waveform will be reset to the zero value at the last time slot.

At the 4-PAM driver block, the value of amplitude of the received MPPM signal is adjusted according to the input odd

bits (Bits1, 3, 5, 7) using a 4×4 MUX. After all, 8-bit data per symbol waveform is transmitted toward the receiver side.

3.1 PLL

The first block in the transmitter is a conventional charge pump PLL. The PLL circuit includes a phase detector, charge pump circuit and voltage-controlled oscillator (VCO). In order to detect the starting point of each time slot, an extra zero detector circuit is also applied to detect the zero value of each time slot. A 5-stage ring oscillator VCO is employed in differential mode to create 5 clock phases and their complement waveforms. It means 10 clock phases with 36º phase difference are produced at VCO block. These clock waveforms (φ1-φ10) are used to produce the proper time slots per symbol (Fig.4(a)).

3.2 Slot selector block

As mentioned before, in the proposed MPPAM method, each symbol is divided into 5 time slots. The value of the modulated waveform is different for each time slot, depending on the value of incoming bits.

To produce 5 equal parts in each symbol, a low power, high speed and simple circuit is proposed, which is shown in Fig.4(b). For example, the first time slot (Sb1) occurs between rising edges of φ1 and φ2 (Fig.4(a)). In the circuit of Fig.4(b), after the rising transition of φ1, when(φ1 =1 ,φ2=0), Q1 and Q2 turn on, the output value will be set to '1'. On the rising edge of φ2, the output node voltage (sb1) will reset to the zero value through the Q3 transistor. As expected, Sb1 is covering 72 degrees.

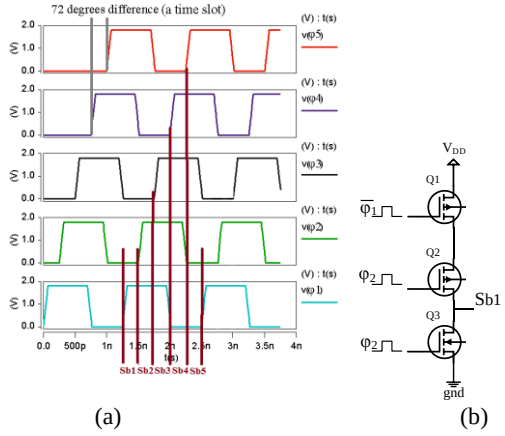


Fig 4. (a) Clock pulses and selected time slots. (b) Slot selector circuit.

3.3 MPPM modulator block

The MPPM modulator block produces the MPPM modulator signal according to the value of input even bits (Bits0, 2, 4, 6). Designing MPPM modulator in voltage mode improves the power dissipation of the transmitter. Fig. 6 shows the proposed simple and low power circuit of MPPM modulator block.

Four slot selector signal in combination with bits 0,2,4,6 are used to form PPM signaling through transistors Q4 – Q19. The last time slot must be equal to zero in differential mode to detect the start point of the next symbol at the receiver block, which is accomplished by Q26 controlled by the last slot selector signal (Sb5).

Transistors Q24 and Q25 make a PMOS latch to keep the previous data before the arrival of new data. Q20 and Q23 in conjunction with R1 and R2 respectively make active inductors. Adding these active inductors add a zero to the transfer function of the circuit, which causes an increase in the circuit speed. Q21 and Q22 which are operated in a linear region are added to obtain high-swing voltage at the output nodes.

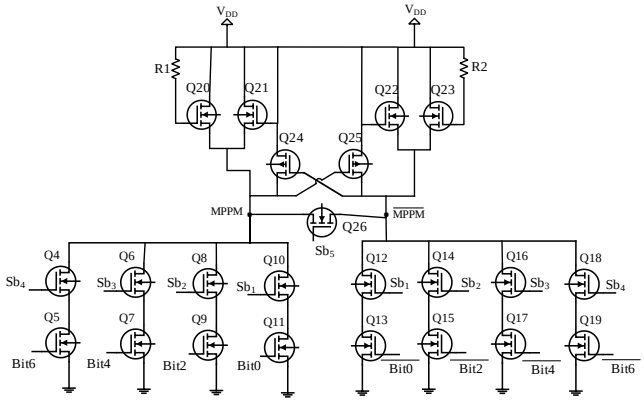


Fig. 5 Proposed MPPM modulator circuit

3.4 4-PAM driver block

The information can be transmitted in two methods: branch currents or nodal voltages of circuits [8] [9]. The first method, current-mode circuits, possesses many unique and attractive characteristics over their voltage-mode counterparts, including a small nodal time constant, high current swing in the presence of low supply voltage, reduced distortion, low input impedance and high output impedance [10] [11]. In current-mode drivers, a constant current drawn from the power supply minimizes the noise injection into both supply and ground. Also, the output current is insensitive to power fluctuation.

In this article, this method is applied to serialize parallel data and provide matching impedance to minimize the reflection at the near end of the channels.

3.4.1 4-PAM driver

MPPM output signal from the last section is used to control the 2-PAM driver. A class AB driver is used to achieve suitable output current swing.

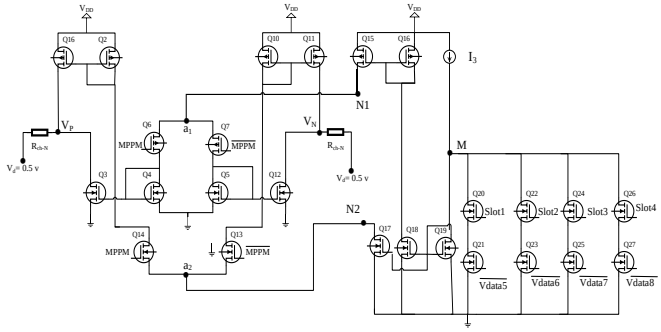


Fig. 6 Generating the additional voltage amplitude in 4-PAM driver.

In the finalizing step, two higher amplitude voltages must be produced according to the values of input odd bits at the

proportional time slots. Fig.6 is used to generate the additional voltage amplitude. A 2-PAM modulator circuit with the presence of its current source depending on the presence of data per time slot is used in combination with a current mode multiplexer. The output of this circuit is paralleled with the output of 2-PAM modulator circuit. Finally, a differential signal with four levels of amplitude at 5-time slots is made according to the values of 8-bit input data.

3.5 Simulation results of transmitter

The proposed MPPAM transmitter is simulated based on TSMC 0.18µm CMOS process model. The eye diagram of the output waveform is indicated in Fig.7. The eye opening width and height are approximately 152Ps ns and 270mV with the peak-to-peak jitter of 35Ps at 8Gb/s data rate frequency. The power consumption of proposed transmitter is 55mW.

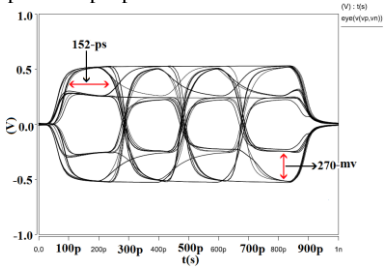


Fig. 6 Eye diagram of the output waveform.

4. Proposed receiver architecture

As shown in Fig.2, 8-bit data and clock signal, which are merged into a single channel, are received at the receiver side. The receiver consists of three main parts including preamplifier, PLL and MPPAM demodulator blocks. The received signal is enhanced by the preamplifier stage before any further process. Ten different phases of clock signal are produced in a differential mode ring oscillator VCO to produce the time slot signals, which are described earlier. Finally, the values of 8-bit data and clock signal are recovered at the MPPAM demodulator block.

4.1 MPPAM demodulator block

The proposed demodulator block consists of 4 comparators for detecting the values of bits 0, 2, 4, 6. In addition, 4 absolute comparators are designed to compare the absolute amplitude of incoming data at different time slots in order to detect the remained 4 bits (Fig. 7).

The absolute comparator circuit is shown in Fig. 8. The dynamic comparator circuit [14] compares the signal which is applied at the gate of M1 with Vref signal. On rising edge of clock signal, the tail transistors will turn on and change the output nodes voltages to the proper values. Transistors Ms1 and Ms2 are added to the circuit to decrease the static power consumption of the circuit [14]. Adding these transistors also help the process of switching outputs.

In the proposed MPPAM modulation, the absolute amplitude of the waveform must be compared to Vref to identify the odd number of bits (bits 1,3,5,7). This task is accomplished using the following equation,

If [V(data+, data-) > V(ref+,Vref-) or V(data-, data+) > V(ref+,Vref-)] then corresponding bit=1 (5)

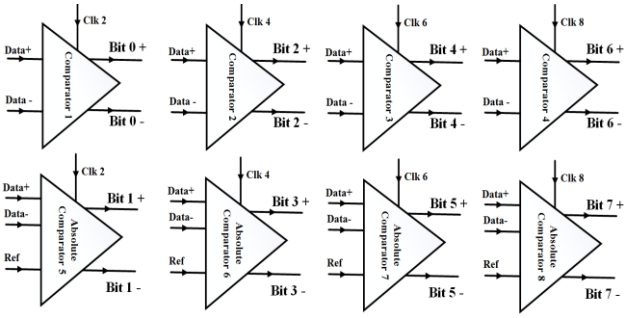


Fig.7. Demodulator block.

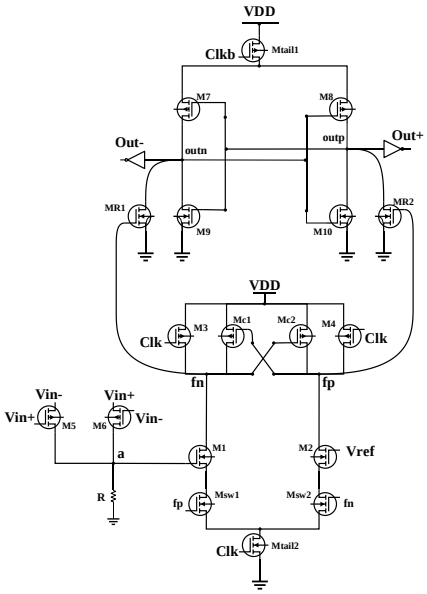


Fig.8 Proposed Absolute comparator Circuit.

In [7], the above equation was implemented using two comparators and one OR gate. However, in the proposed circuit, the above equation is achieved by adding two transistors M5, M6 and R resistor to a single comparator. Therefore, the number of comparators is decreased considerably in comparison to [7].

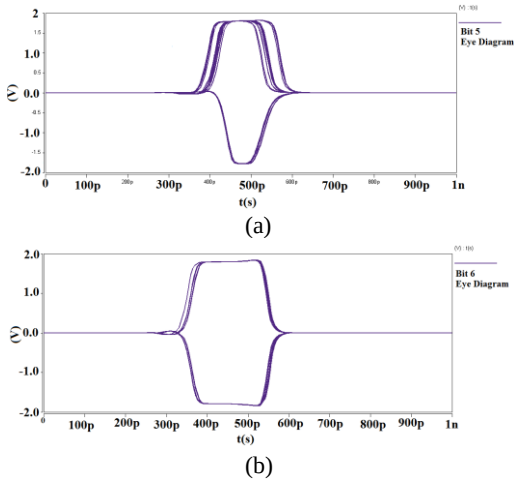
As can be seen in Fig.8, a larger amount of Vin- and Vin+ will pass and present at node a. This value is compared to Vref to indicate the values of bits 1,3,5,7 according to the clock phases applied as the clock signal.

A 0.5m serial advanced technology attachment (SATA) line is used between the transmitter and receiver as a channel.

4.2 Simulation results of the receiver

The eye diagram of recovered odd bits (bit 5) is presented in Fig.9(a). The value of peak–to-peak jitter of the recovered data is obtained as 40ps. Fig. 9(b) indicates the eye diagram of recovered even bits (bit 6). The value of peak-to-peak jitter is obtained as 14ps. The power consumption of receiver is 15mW. Table 1 presents a comparison between the proposed transceiver and previous work. As can be seen, the proposed modulation resolves 8 bits plus clock per 5- time slot which are the greatest.

It also achieves the highest bit rate per symbol in comparison to others.



(a)

(b)

Fig. 9. (a) The eye diagram of recovered (a) odd bits (b) The eye diagram of recovered even bits

Table 1. A comparison between the proposed transceiver and previous work

References	[4]	[6]	[7]	This work
Technology (µm)	0.18	0.35	0.18	0.18
Supply Voltage (V)	1.8	3.3	1.8	1.8
Bit Rate	1Gb/s	3.2Gb/s	7Gb/s	8Gb/s
Clock Rate	250MHz	800 MHz	1GHz	1GHz
Modulation Technique	PWAM	PWAM	PWAM	Proposed MPPAM
Existed data in channel	4-Bit Data+Clock	4-Bit Data+Clock	7bit-data+clock	8bit-data+clock
Power Consumption	Rx:45mW Tx:86mW	Rx:35mW Tx:220mW	Rx:14mW Tx:71mW	Rx: 15mW Tx:55mW
Value of Jitter (Recovered data P-P)	107Ps	21Ps	42.6Ps	40Ps
Results	Measured	Simulated	Simulated	Simulated

5. Conclusion

A new multi- pulse position amplitude modulation (MPPAM) was proposed in this paper. In this structure, the advantages of MPPM and PAM technologies were combined to improve the quality of communication. By transferring 8 bits per 5-time slots per symbol, the total bandwidth per symbol was increased. Additionally, due to the presence of the 5th time slot, which was dedicated to the clock signal, the clock was embedded in the data stream and the need for a complicated CDR at the receiver side was mitigated. In the proposed structure, the value of minimum pulse width (PW) was significantly larger than the conventional non-return to zero data PW (Tb). Therefore, the value of ISI in the channel improved considerably. In the proposed transceiver, the symbol rate was 1Gb/s and the equivalent data rate was 8Gb/s.

6. References

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