Single-Phase STATCOM with Multilevel U-Cell Converter

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Abstract

This paper presents a control algorithm and its implementation on a grid connected single phase multilevel U-cell converter for reactive power control. The sinusoidal pulse width modulation is used for the control of five-level voltage source converter. The phase angle of grid voltage is obtained by using a single-phase phase-locked loop and two modulation signals are compared with a single carrier wave in order to control the IGBTs. The orthogonal voltage waveform which has 90 degrees phase shift with respect to source voltage is generated by using a second order generalized integrator. The implementation of the proposed controller has been carried out in the laboratory by using TMS320F28335 floating point digital signal processor.

1. Introduction

The performance of AC power system depends on the power quality measures [1]. The reactive current should be compensated at the load side in order to fulfill the line current capacity with active current. The traditional solution of the reactive power compensation has been implemented by using the capacitors or inductors connected in parallel to loads [2]. However, the development of power semiconductor technology in high power application has enabled the usage of static synchronous compensator (STATCOM) [3,4] to generate or absorb required reactive power demand. This application reduces the response time, eliminates voltage spikes and attenuates the current harmonics when it is compared to traditional solution.

The multilevel converters are preferred circuit topologies in the STATCOM applications [5, 6]. The serial connection of semiconductors and the availability of modular designs have created a wide spread use of these multilevel converters at high voltage and high power applications. The cost of the converter can be reduced by using the optimized multilevel structures. The cross-connected U-Cell converter given in Fig. 1 has higher efficiency than the H-bridge topology [7] since it has less number of power switches and associated drive [8, 9].

The common switching methods for multilevel converters are implemented either at the fundamental frequency with specific harmonic elimination or at high switching frequency with pulse width modulation (PWM) techniques. The switching frequency is an effective parameter on the switching losses of solid state devices. Although the power loss decreases as the switching frequency decreases, the total harmonic distortion of the line current is reduced with the PWM techniques. The level shifted carrier based sinusoidal pulse width modulation (SPWM) method has been implemented in the multilevel converters [10]. The capacitor voltage balancing is an essential part in control algorithm for the multi-level converters and it affects the harmonic content of the output voltage and line current [11]. The DC capacitor voltage levels are regulated by the PI controllers whose output is the reference signal for power angle (phase difference) between the grid and converter output voltages. The real energy storage and capacitor voltage levels are controlled by the power angle.

There are several methods proposed and implemented in order to control the reactive power [12, 13]. The orthogonal voltage is generated by the second-order generalized integrator (SOGI) [14, 15]. The reactive power is estimated by taking the time average of the waveform generated from the multiplication of the orthogonal voltage and grid current.

The rest of the paper is organized as follows: Section 2 gives the detail of the reactive power estimation based on the single-phase PLL and the SOGI. The programming algorithm prepared for the digital signal processing unit (TMS320F28335) is described in section 3. The simulation results of Matlab are compared to the experimental ones in section 4 and the conclusion is given in section 5.

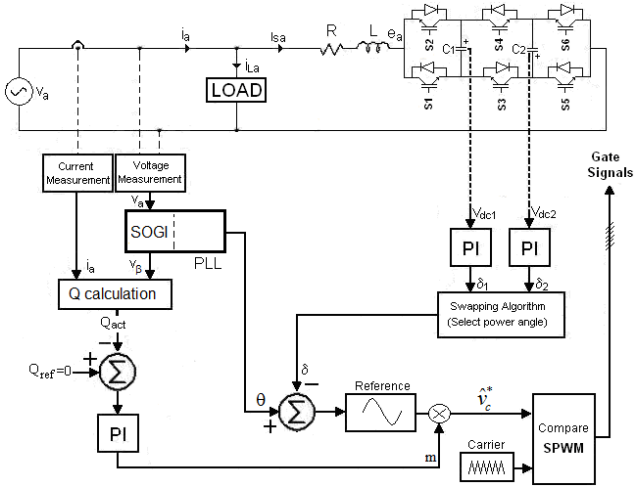

Fig. 1. Block diagram of reactive power control

2. Single Phase PLL and Reactive Power Calculation

A single-phase PLL topology requires two inputs which are the in-phase and its orthogonal components of source voltage in order to extract the phase information of source voltage. A three-phase PLL method is based on Clarke and Park transformations, where three-phase supply voltages are transformed to the orthogonal two-phase voltages at the stationary reference frames by using the Clarke transform (C_T). The orthogonal component of source voltage in a single phase system can also be generated by using the second order generalized integrator (SOGI) having the transfer function given below [15];

$$H(s) = \frac{s.\omega}{s^2 + \omega^2} \tag{1}$$

The block diagram of the SOGI in z-domain is obtained by using the Euler backward integrator and it is given in Fig. 2 [16]. The magnitude and phase of input fundamental voltage are retained at the output v_α , while its orthogonal component v_β has 90 degrees phase shift and it is available from the SOGI at the labelled terminal in Fig. 2.

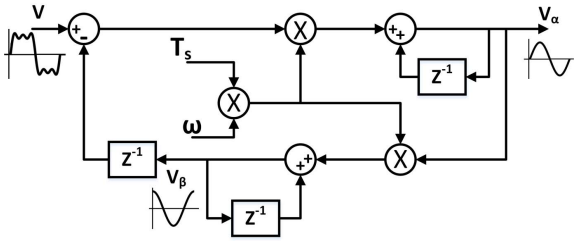

Fig. 2. Second order generalized integrator (SOGI)

The park transformation is applied on the in-phase voltage v_α and the orthogonal component v_β . The transformation from stationary reference frame to synchronously rotating reference frame is carried out in (2);

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{2}$$

$$\theta(\xi) = \int_0^t \omega(\xi) d\xi + \theta(0) \tag{3}$$

The speed of synchronously rotating reference frame is fixed to the supply frequency ($\omega(\xi) = \omega$) . The quadrature component v_q becomes zero when the d-axis is initially aligned with the peak of the fundamental component of v_α . Therefore, the quadrature component of voltage v_q is compared to zero reference and the error is passed through PI controller. Then the phase angle θ of input voltage is estimated from the integral of ω as it can be seen in Fig. 3.

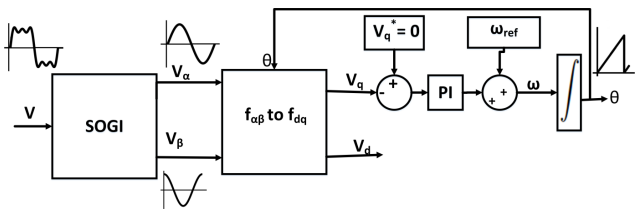

Fig. 3. The block diagram of single-phase PLL

The reactive power of single phase system is computed by using the time-average of the instantaneous multiplication of the line current i_α and the orthogonal component voltage v_β available from the SOGI.

$$Q = \frac{1}{k.T} \int_\tau^{\tau + k.T} i_a . v_\beta \, dt \tag{4}$$

Where " k " is an integer number for the pre-specified integration interval and T is the period of the supply voltage. It should be noted that the SOGI estimates the fundamental component of source voltage by using the transfer function in (1).

The complete block diagram of a reactive power control in a single phase system is given in Fig 1. In this system, there are two capacitors in the AC to DC converter hence the voltage balancing is performed by using the swapping algorithm. The control signal $\hat{v}_c^*$ for the PWM operation can be generated by using the phase angle θ of the source voltage, the power angle δ estimated at the output of dc link PI controller and modulation index m estimated at the output of another PI controller employed for reactive power compensation.

$$\hat{v}_c^* = m\sin(\theta - \delta) \tag{5}$$

The AC to DC converter is operated to generate five-level voltage at the grid side. The gate signals of six IGBTs are generated according to the logic given in Fig. 4 by using (5) and its shifted form at the value of V_{tri} . In this logic, two sinusoidal control voltages are compared to the single triangular wave. It should be noted that the pairs (S1, S2), (S3, S4) and (S5, S6) work in complementary logic.

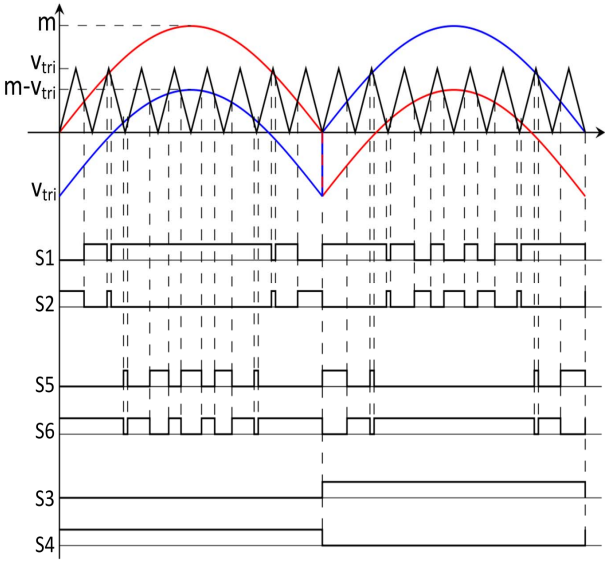

Fig. 4. Switching logic of single phase 5-level converter

3. Flowchart of the program on the DSP

The software has been programmed in C++ compiler/linker which is named as Code Composer Studio (CCS) for TMS320F28335 floating point DSP. The program on the DSP is organized in two parts: The first part has the main loop in which the ADCs, PWM ports, interrupts and other initialization routines are set up. The second part consists of all the control algorithms (estimation of reactive power, PLL and PI controllers, etc.).

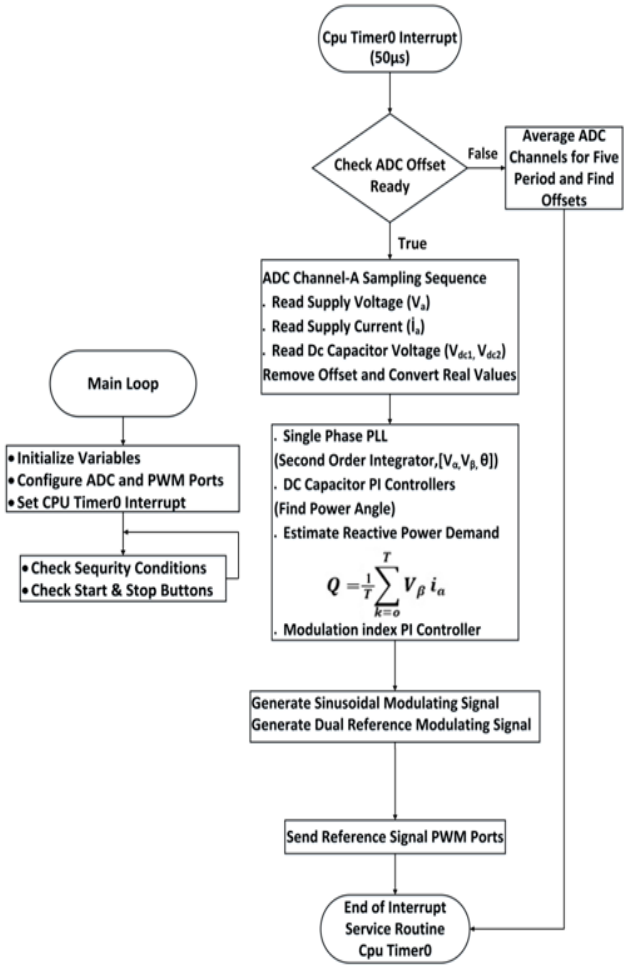

Fig. 5. The flowchart of the program on the DSP

The offset values of the ADC channels have been calculated during the start-up of DSP by using the average values. The average value of the AC voltage and current received via the ADC channel is estimated over five periods. This offset also covers the op-amp tolerances of signal conditioning circuit. Since the expected average value of them is zero, their calculated values are subtracted from the data read from ADC during the operation. ADC channel group A sampling sequence is reserved for reading the supply voltage, supply current and DC link voltages. The phase information θ of supply voltage is used for controlling the swapping algorithm of DC capacitor voltages. The phase difference δ which has been generated by the dc link PI controller is added to θ which is estimated by the PLL in order to obtain a sinusoidal reference signal with unity magnitude. The magnitude of this signal is multiplied by the modulation index m received from the PI controller of reactive power. The flowchart of the DSP program is given in Fig. 5.

Five-level PWM output voltage can be generated at the grid side of AC to DC converter by comparing four triangular carrier signal with a sinusoidal reference signal. However, in the DSP used here, there is one triangular carrier signal generated by the internal structure and its level is fixed. Therefore, two identical reference signals shifted by a magnitude of V_{tri} shown in Fig. 4 have been compared with one triangle wave in order to generate the SPWM switching signals through the PWM ports.

A triangular carrier signal is generated by setting one timer of DSP. The frequency modulation ratio can be controlled by adjusting the frequency of carrier signal in DSP. It should be noted that when the modulation ratio is chosen as an odd integer, converter output voltage becomes half-wave symmetric. Hence, the even harmonic components are not disappeared on converter output voltage at grid side. The carrier frequency has been selected at 4950 Hz providing the half-wave symmetry on converter output voltage.

4. Results

The system is simulated in the Matlab/Simulink and tested on the single phase five-level STATCOM in the laboratory. The supply voltage is set to 130 volts RMS via single phase autotransformer and the reference voltage for each capacitor is set to 100 volts DC. The converter is connected to grid through 5 mH switching inductor and it has two 10000 µF DC link capacitors with 22 kΩ discharge resistor. The experimental results are recorded by Lecroy wave runner 604ZI oscilloscope and energy analyzer Fluke 434.

A load having the resistor of 900 W and the reactor of 900 VAR are connected in parallel to the AC power source after the STATCOM is operated at no-load and its dc capacitor voltages are stabilized. When the R-L load is switched on, the supply current rises from a low level required for holding the dc capacitor voltages constant to the level of 10 A demanded by the load. Fig. 6 and Fig. 7 show the simulation and experimental results of the R-L loads connected in parallel to single phase converter. The experimental and simulation results are not synchronized at the instant when the load is connected to the source voltage. The supply voltage and source current are in phase after few cycles. The RMS magnitude of STATCOM voltage is greater than the supply (grid) voltage. Hence, STATCOM current leads supply voltage by 90 degrees. It takes almost 100 ms to damp out the whole transients. This transition time depends on load time constant, the instantaneous value of source voltage applied when the load is switched on and response of STATCOM. It is clearly seen that the source current is in-phase with source voltage after almost one period (20 ms) which is the computational delay of required reactive power. Also, it is observed that as the load current is increasing during this transition, the value of STATCOM current increases and retains the power factor one.

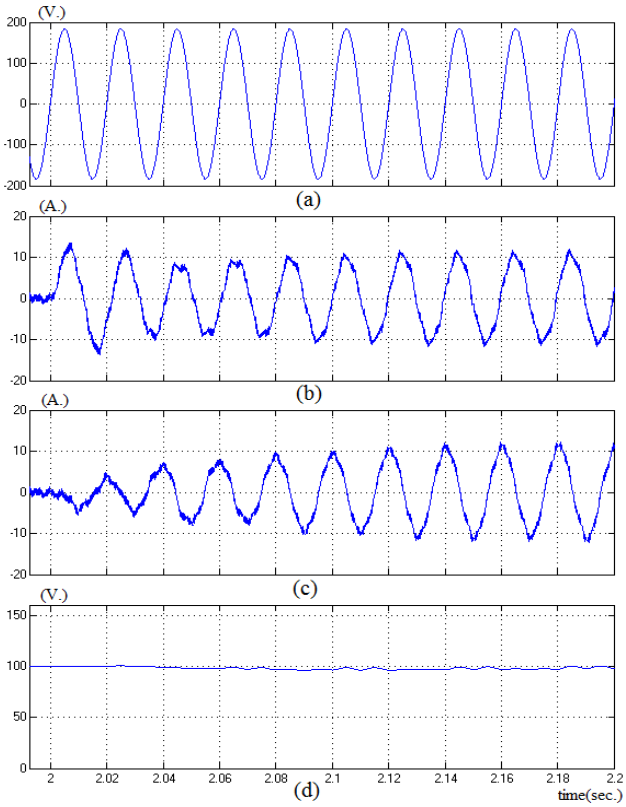

Fig. 6. Simulation result of R-L load a) supply voltage b) supply current c) STATCOM current d) capacitor voltage

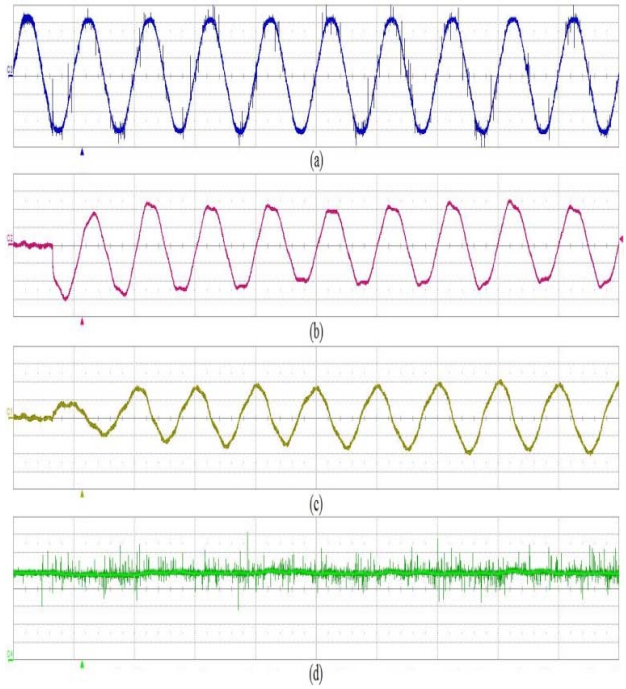

Fig. 7. Experimental result of R-L load a) supply voltage (50V/div) b) supply current (5A/div) c) STATCOM current (5A/div) d) capacitor voltage (20V/div), (time axis: 20 ms/div)

Fig.8 and Fig. 9 show the simulation and experimental results of the resistive (900 W) and capacitive (900 VAR) loads connected in parallel to the STATCOM. The source voltage and source current are in phase again after around four periods (80 ms). In the R-C loading, the RMS value of STATCOM voltage is lower than the supply voltage, hence the STATCOM current lags supply voltage by 90 degrees and supply current becomes in phase with supply voltage. It is observed that there is almost % 4 fifth order harmonic on source voltage during the experimental work, therefore that much of harmonic component has been added to the source voltage during Matlab simulation. When the inductive loading in Fig. 7 and capacitive loading in Fig. 9 are compared during the starting transients, it is clear that the time required to reach at steady-state from no-load operation is longer in capacitive case. The reason for that the variation of modulation index m which is the output of reactive power PI controller is taking a longer time in the capacitive case. This settling time depends on the magnitude of voltage drop on source impedance and switching inductance. The STATCOM voltages at no-load and at inductive loading are not far away from each other, therefore the variation of modulation index in inductive loading settles down faster than that of the variation in capacitive case.

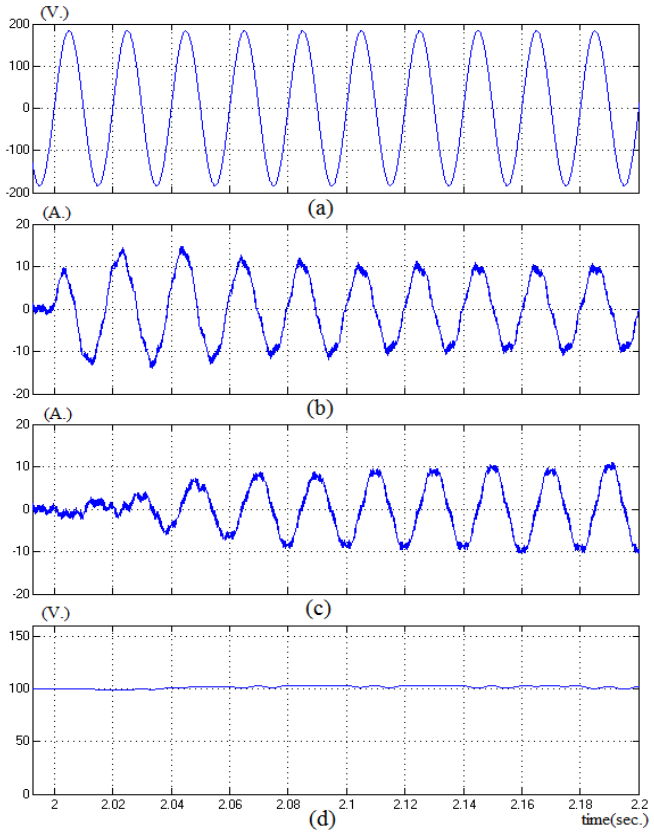

Fig. 8. Simulation result of R-C load a) supply voltage b) supply current c) STATCOM current d) capacitor

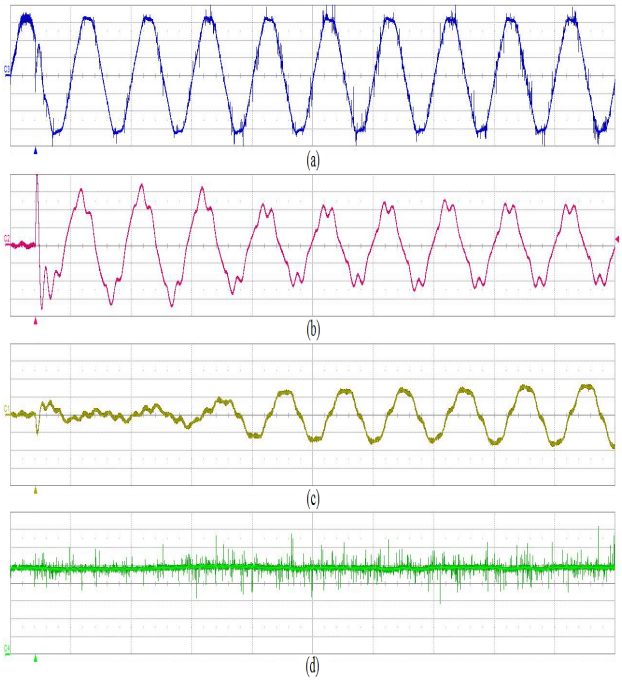

Fig. 9. Experimental result of R-C load a) supply voltage (50V/div) b) supply current (5A/div) c) STATCOM current (5A/div) d) capacitor voltage (20V/div), (time axis: 20 ms/div)

5. Conclusions

The five-level AC to DC converter used here has less number of switches and associated drive circuit than conventional cascade H-bridge converters. The level shifted carrier based SPWM is implemented on five-level converter by using two reference signals and one carrier waveform. The synchronous reference frame based single-phase PLL and the second order generalized integrator are implemented on the DSP. The SOGI as a part of PLL tracks the source voltage to extract its orthogonal component. This simple control algorithm uses less programming capacity on microcontroller than the demand of single phase p-q and non-active current methods. The simulation and experimental results on R-C and R-L loads verify that the proposed converter compensates the reactive power properly.

References

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