A New Bridgeless Multilevel Inverter Structure with Reduced Number of Power Switches

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Abstract

Multilevel inverter (MLI) has been a different alternative instead of traditional two level inverters and commonly used to obtain quality output voltage with lower Total Harmonic Distortion (THD). In addition, outstanding advantage of MLI is reduced voltage stress of the power switches. However, the structure of MLI needs excessive number of power switches especially for the higher level inverter that supplies lower THD value and lower voltage drop on the semiconductor switches. In this paper, new bridgeless multilevel inverter structure with reduced number of power switches has been proposed. Additionally, the working operations of proposed MLI have been analyzed. Harmonic Minimization Pulse Width Modulation (HMPWM) technique has been applied to proposed MLI and simulation results have been obtained by using Simulink&MATLAB. Simulation results have clearly proved that proposed new MLI's structure can be operated with resistive and inductive load and generate waveform output voltage of traditional MLI by using less number of power switches.

1. Introduction

In recent years, inverter technologies have been widely used and have extensive researches in power electronics' working area. Especially, developing semiconductor technology and different modulation techniques make power electronics application more practicable and efficient. However, in high power and medium voltage, the voltage stress of the power switches is extremely high. For this reason, multilevel inverters (MLIs) are a different alternative to traditional inverters with some advantages such as lower voltage drop on switches; low distorted input currents, lower Total Harmonic Distortion (THD) in output voltage [1].

Generally, there have been three types of MLI's structure; Cascaded H-bridge topology, Diode-Clamped topology, Capacitor-Clamped topology. For the first time, Cascaded H-bridge multilevel inverter structure including serial connection of H-bridge modules was introduced in 1975. After that time, other suggested topologies were developed respectively. The most suffered disadvantageous of Diode-Clamped and Capacitor-Clamped topologies are necessity of large number components in the hardware. Especially, with higher level the number of blocking diodes rises exponentially. Also, diode-reverse recovery is another problem in Diode-clamped topology. Similarly, Capacitor-clamped topology has a large number of bulk capacitor in order to balance charging and needs well-selected clamped capacitor combination [2, 3]. Fortunately, Cascaded H-bridge topology doesn't need extra diodes or capacitor to generate stepped output voltage. Implementation of Cascaded H-bridge topology is more practical and lower costed when compared with clamped topologies [4].

The most important advantages of MLIs are low THD in output voltage and low voltage stress on the power switches when compared with traditional inverter. Additionally, THD can be reduced by increasing the level number. Therefore, the quality of output voltage increases. However, increasing level means more components such as power switches, gate drivers and DC sources. In order to decrease the number of power switches and cost of MLIs, many researches on multilevel inverter using less number of switches [5-10] have been done. In [5], researchers have proposed cascaded Half-bridge multilevel inverter structure and analyzed in detail. A new multilevel structure in [6], have cascaded level modules with bidirectional switches conducting the current in each directions. Researchers in [7] have come up with a different multilevel inverter topology, and studied working operations and current direction for 5-level output voltage. Similarly in [8], different MLI topology have been developed and experimental analyzes have been given for five level output voltage. A new configuration of cascaded MLI have been proposed, with simulation studies stepped output voltage have been obtained [9]. Finally in [10], a 7-level module have been developed and analyzed in detail. These developed model of MLI needs less number of power switches with some advantages such as controlling of load current, necessity of less gate driver, modularity etc. However, all topologies in [5-10] have the H-bridge inverter at the output of cascaded level module. For this reason, in this study, new bridgeless multilevel inverter structure with reduced number of power switches has been proposed. In Fig.1, a comparison including the all multilevel inverter topologies using less number of switches, Cascaded H-bridge topology and proposed MLI's structure have been done.

As illustrated in Fig.1, excepting proposed structure, [7-9] have less number of power switches and [10] need more isolated DC sources. Fortunately, the proposed structure needs both lower power switches and isolated DC sources than [5-10]. The second line of the figure gives the number of isolated DC sources in the suggested MLI topologies. Each DC sources' value in proposed structure change with the number of level and have been mentioned in next Section.

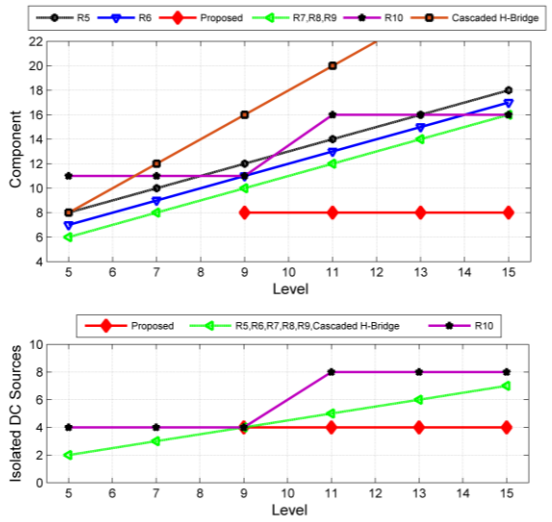

Fig. 1. Number of components and isolated DC sources for all conventional multilevel inverter structures

This paper is organized as follows; in Section 2, the proposed multilevel structure, level modules and working operations have been analyzed in detail. Modulation techniques that can be applied to proposed MLI have been analyzed in Section 3. In Section 4, simulation results have been given for 9-level inverter. Conclusion is presented in Section 5.

2. Proposed Multilevel Inverter Structure

The proposed multilevel inverter has been given in Fig.2. As seen in the figure, proposed MLI doesn't have H-bridge inverter and includes series connection of level modules. All level modules have same structure with different connection port as seen in Fig.3.

Proposed MLI has Half-bridge modules as in [1,5]. However, value of DC sources and connection ports of the each level module change with the number of level desired to obtain at the output. So as to get 9-level output voltage, two positive modules and two negative modules are needed and 9-level structure has been illustrated in Fig.2. In addition, 13-level output voltage can be obtained by 9-level connection strategy. But, the switching strategies and value of DC sources are different. For 11 and 15-level output voltage, 1st, 2nd and 3rd level modules must be linked in series by considering positive connection port of the modules. 4th module has negative connection port in order to get 11 and 15-level output voltage. In Table 1, the value of DC sources and connection ports of the level modules needed for each level are given.

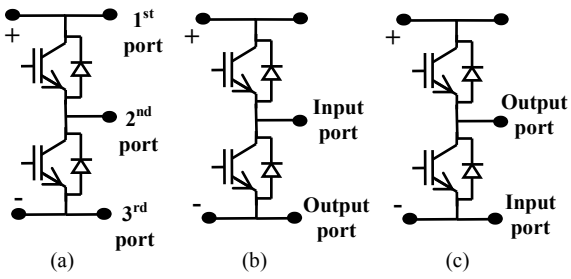

Fig. 3. a) Level module, **b)** positive connection port, **c)** negative connection port

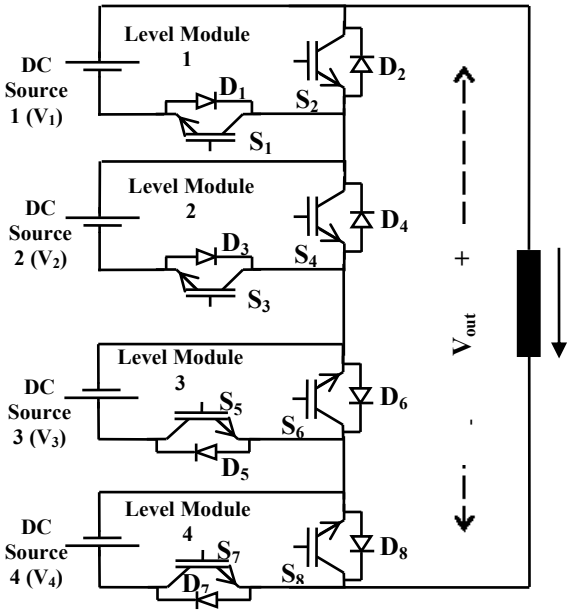

Fig. 2. Proposed new multilevel inverter structure for 9 and 13-level output voltage

Table 1. Value of isolated DC sources and connection ports of level modules for all level between 9 and 15

Number of level	Number of connection ports		Value of isolated DC sources				Output voltage	
	Positive	Negative	V_1	V_2	V_3	V_4	max	min
9	2	2	V_{DC}	$3V_{DC}$	V_{DC}	$3V_{DC}$	$4V_{DC}$	$-4V_{DC}$
11	3	1	$2V_{DC}$	$3V_{DC}$	V_{DC}	$4V_{DC}$	$5V_{DC}$	$-5V_{DC}$
13	2	2	$4V_{DC}$	$2V_{DC}$	V_{DC}	$5V_{DC}$	$6V_{DC}$	$-6V_{DC}$
15	3	1	V_{DC}	$2V_{DC}$	$4V_{DC}$	$8V_{DC}$	$7V_{DC}$	$-7V_{DC}$

As seen in Table 1, proposed multilevel inverter structure can supply all output level between 9 and 15 with different combination of connection port and isolated DC sources. Proposed MLI has symmetrical output voltage waveform. However, DC sources' the value may not be the same and changes based on number of level. In order to obtain 9-level output voltage given in Fig.4, proposed structure needs four isolated DC sources and two DC sources are three times of the others. 11, 13 and 15-level output voltage can be obtained by using different DC sources' values by considering Table 1.

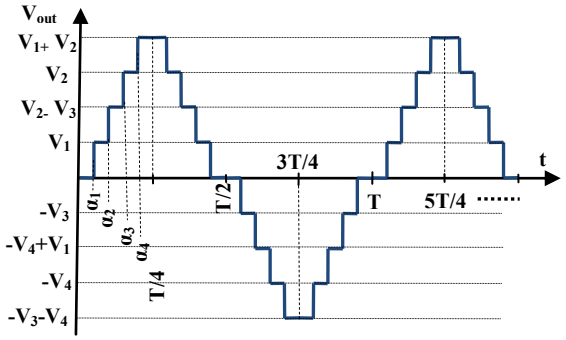

Fig. 4. Output voltage of 9-level inverter

Table 2. The output voltage and direction of current as to switching states defined for all working operations of proposed 9-level inverter

	States of switches								Voltage	Current
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_L	$İ_L$
1		on		on		on		on	0	+
2		on		on		on		on	0	-
3	on			on		on		on	V_1	+
4	on			on		on		on	V_1	-
5		on	on		on			on	V_2- V_3	+
6		on	on		on			on	V_2- V_3	-
7		on	on			on		on	V_2	+
8		on	on			on		on	V_2	-
9	on		on			on		on	V_1+V_2	+
10	on		on			on		on	V_1+V_2	-
11		on		on	on			on	-V_3	+
12		on		on	on			on	-V_3	-
13	on			on		on	on		-V_4+V_1	+
14	on			on		on	on		-V_4+V_1	-
15		on		on		on	on		-V_4	+
16		on		on		on	on		-V_4	-
17		on		on	on		on		-V_3-V_4	+
18		on		on	on		on		-V_3-V_4	-

In Table 2 and Fig.6, switching strategies have been given for 9-level output voltage in detail. States of power switches in each level module cannot be the same because of the short circuit. Actually, there are nine switching states in order to get 9-level output voltage. The other states are the same but the direction of the current are opposite as seen in Fig.6.a and Fig.6.b. For resistive load, it is clear that power flows from source to load. However, for inductive load the direction of the current changes transiently. For this reason, other working operations where power flows load to sources have been illustrated.

For Fig.6.a and Fig.6.b, output voltage is 0. Positive load current flows towards S_8, S_6, D_4 and D_2. However, direction of negative load current is S_2, S_4, D_6 and D_8 in turn.

Fig.6.c and Fig.6.d illustrates the direction of current for V_1 which is second step of the output voltage as seen in Fig.4. Positive load current flows through S_8, S_6, D_4 and S_1. While current is negative, the state in Fig.6.d, that is also regenerative mode, is used.

The third step of the output voltage (V_2-V_3) can be obtained with the state given in Fig.6.e and Fig.6.f. The current flows towards S_8, D_5, S_3 and D_2 if the current is positive. For the energy regeneration mode given with Fig.6.f, direction of current is through S_2, D_3, S_5 and D_8. The other working operations can be deduced by analyzing Table 2 and Fig.6. In addition to this, the all regenerative working mode, where the energy regeneration becomes, can be investigated by analyzing Fig.6.d, Fig.6.f, Fig.6.h, Fig.6.j, Fig.6.k, Fig.6.m, Fig.6.o and Fig.6.r.

3. Switching Strategies for Minimization of Total Harmonic Distortion

Switching strategies, also known as modulation techniques can be classified into two categories; fundamental frequency and high switching frequency. The modulation techniques using high switching frequency are Space Vector Pulse Width Modulation and Sinusoidal Pulse Width Modulation. Especially at high level and high switching frequency, the modulation techniques are complicated. This make the modulation techniques inconvenient for practical implementation [2].

There are several practical techniques used for minimizing of THD such as Harmonic Minimization Technique [3, 7, 11], Optimization Algorithm based Harmonic Minimization Technique [11] and Selective Harmonic Elimination Technique (SHE)[1]. However, with high level number, the number of SHE equations increases. Thus, solving of nonlinear SHE equations becomes more difficult. In addition, SHE technique eliminates low order harmonics, THD would not be reduced and filter at the output would be required. These are disadvantages of SHE technique. However, with any the qualified optimization algorithm SHE technique is a very effective especially at high level number with a large number of eliminated harmonic components [4]. Similarly, Optimization Algorithm based Harmonic Minimization Technique is a very effective method to minimize THD. This method solves the THD equation, get the switching angles (α_1, α_2, α_3, α_4) and look for at which modulation index minimum THD occurs [3, 7, 11].

Therefore, in this paper, Harmonic Minimization Technique that is not time consuming and simpler than suggested minimization techniques have been implemented to analyze working operations and switching strategies of new proposed multilevel inverter structure.

4. Simulation Results

In this study, Harmonic Minimization Technique has been applied to proposed new bridgeless multilevel inverter structure with reduced number of power switches. The fundamental frequency of output voltage is 50 Hz. Results of 9-level output voltage including resistive and inductive load has been given to demonstrate performance of proposed topology. Simulations have been developed by using Simulink&MATLAB. In Fig. 5, simulation bocks of proposed multilevel inverter have been given. The pure resistive load is 1 ohm and inductive load is 1 ohm and15mH connected in series.

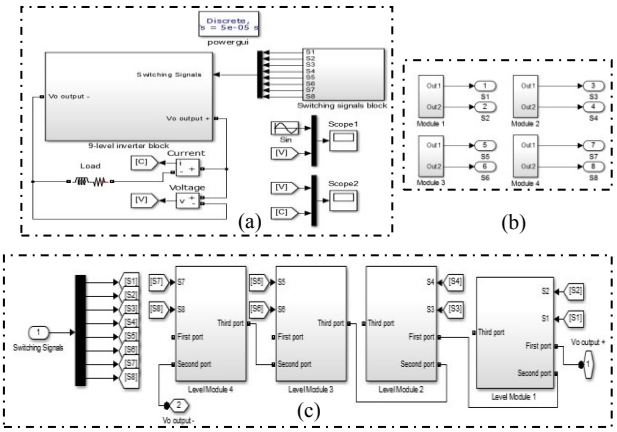

Fig. 5. Simulation blocks of proposed multilevel inverter structure, a) General scheme, b) Switching block, c) 9-level inverter block

Fig. 7 shows 9-level output voltage having four equal voltage step both positive and negative side of the output. The maximum rate of output voltage is 400V and the minimum voltage of output is -400. While output current for resistive load is stepped, inductive current is sinusoidal with phase angle.

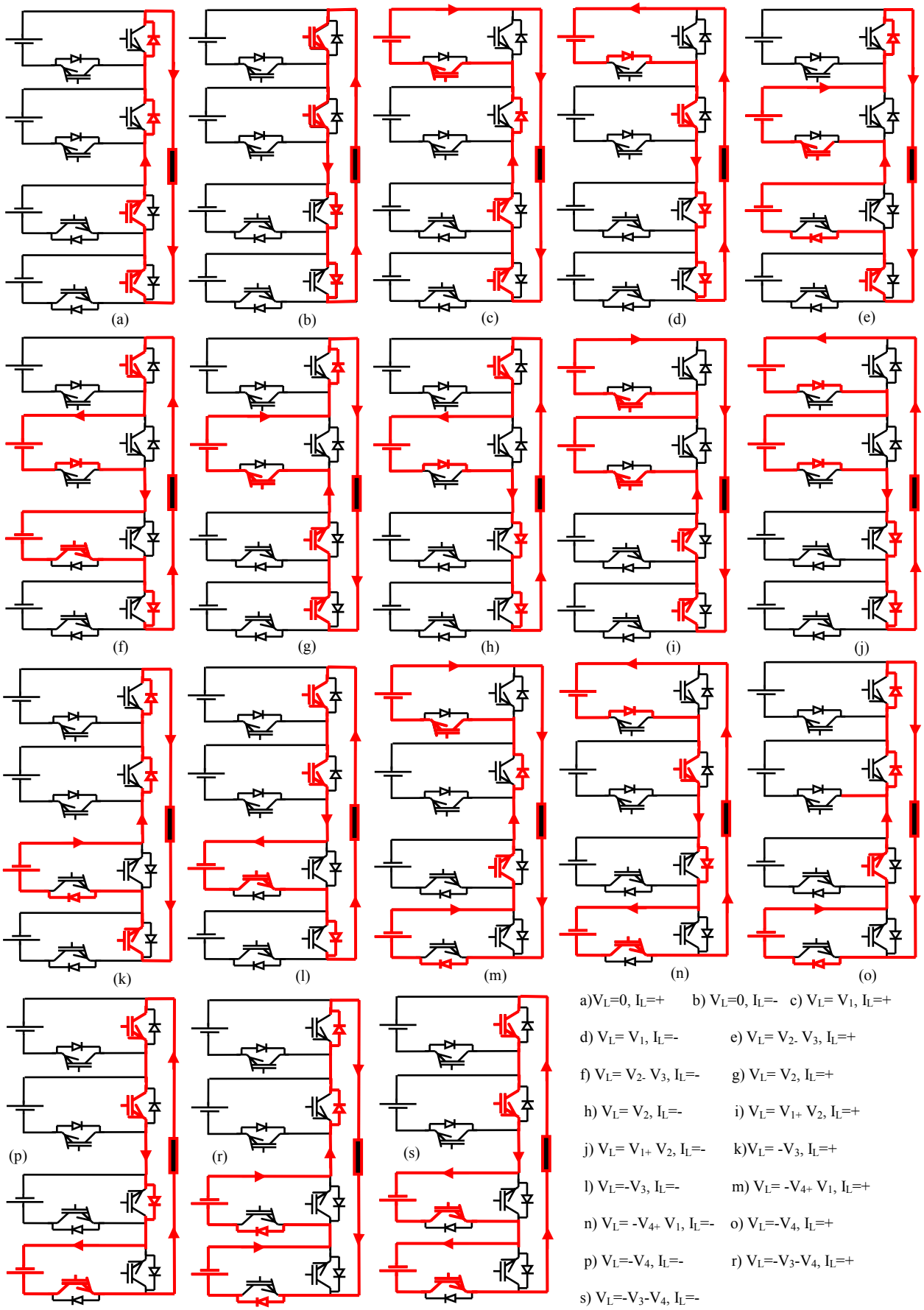

Fig. 6. The working operations of 9-level inverter

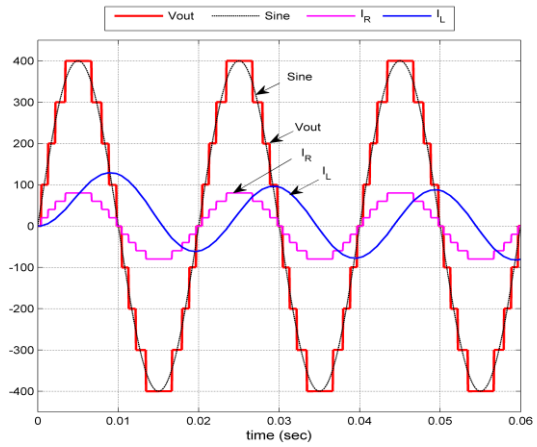

Fig. 7. Output voltage, currents of pure resistive (R) and inductive load (series R-L) for 9-level inverter

The sine signal and output voltage intersect at half of the each step which is aim of Harmonic Minimization Technique to make output voltage waveform similar to pure sinusoidal waveform and obtain low THD value.

Gate signal of 9-level output voltage are given with Fig. 8. It is clear that 10 cycle of the switching operation are illustrated in this figure because of output voltage with 50 Hz and 0.02 seconds period. The other switching signals S_2, S_4, S_6 and S_8 are conjugated of S_1, S_3, S_5 and S_7 respectively.

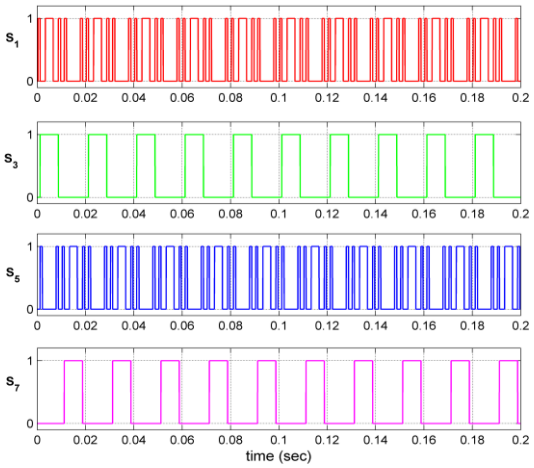

Fig. 8. Switching signals of 9-level inverter

It is understood that by applying proposed switching strategy to the proposed multilevel inverter, both resistive and inductive current can be obtained easily. Harmonic Minimization Technique can be applied proposed multilevel inverter structure. Therefore, it can be concluded that proposed multilevel inverter is compatible with the other modulation techniques suggested in before. Because, the other modulation techniques need uniform number of switching angles with each switching frequency. For this reason, the other modulation techniques can be adapted to proposed bridgeless multilevel inverter with reduced number of power switches.

5. Conclusion

In this study, a new bridgeless multilevel inverter structure with reduced number of power switches has been proposed and analyzed in detail. Introduced multilevel inverter can produce 9, 11, 13 and 15-level output voltage with four level modules including different connection port. The working operations and switching strategies for 9-level inverter have been given in detail. The proposed multilevel inverter have been compared with others using reduced number of switches. Number of power switches and DC sources are lower than similar studies. Simulated multilevel inverter have been loaded both pure resistive and inductive load. Results have apparently demonstrated that new bridgeless multilevel inverter with reduced number of power switches can be effectively used with pure resistive and inductive load, Harmonic Minimization Technique can be easily applied to proposed multilevel inverter structure.

6. References

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