

Three-Phase Interleaved Boost DC/DC Converter with High Voltage Gain and Reduced Nominal Value on Power Devices

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Abstract

In this paper, a new interleaved boost dc-dc converter is presented for PV applications. The proposed converter consists of three-phase which are parallel connected to each other. There are voltage multiplier units between the phases for increasing the output voltage. By increasing the voltage multiplier units (by connecting the series together), the output voltage will be more increase. In addition, the nominal value of the power components is reduced. Therefore, the voltage stress of switches and diodes for various duty cycles is low and so, the efficiency is high. One of the other advantages of the proposed converter input current ripple is low with the utilization of interleaving techniques. These advantages cause the proposed converter to be a good candidate for PV panels. To illustrate the merits of proposed converter, comparison results with other converters are provided. Also, theoretical analysis for two stages with operating at 25kHz is provided.

1. Introduction

Nowadays, electric energy generation based on wind turbines, fuel cells and photovoltaic (PV) technologies has attracted great attention. However, the output voltage of these sources is relatively low. To solve this problem, dc-dc converters with high voltage conversion ratio are a suitable choice [1-5]. A non-isolated dc-dc converter with high voltage conversion ratio and low voltage stress across power switches have been proposed in [6]. In this topology by increasing the turn's ratio of the used diode-capacitor-inductor unit (D-C-L). This topology can generate a high voltage gain significantly. However, this converter has problems which limit their application in renewable energies or high power level. Therefore, in order to apply the renewable applications or high power levels and to increase the overall efficiency of the structure, should decrease the number of power devices. In addition, the number of inductors is higher which leads to use more core, so the cost of the converter will raise. In [7], a high step-up DC-DC converter is presented for PV applications. The efficiency of proposed converter is good but this topology is not suitable for high power levels. In fact, by increasing the current level and voltage level, the nominal values of power components will increase and leads to increase the normalized voltage of semiconductors. In [8], an isolated DC-DC converter for renewable energy applications has been proposed. This converter consists of an interleaved DC-DC converter and PV panel which connected to the one transformer for the controllable switch in each phase. This converter is applied for simultaneous maximum power point tracking (MPPT) control of

the wind and two different PV panels. This topology has higher normalized voltage stress across power switches and power diodes. Therefore, this topology not suitable for high power levels because the cost of power component will higher. In [9], non-isolated dc-dc converter boost based on switched-capacitor/switched-inductor is proposed which it can provide high step-up voltage conversion ratio. But with increasing of high voltage and current stress, high duty-cycle operation, and limited dynamic response. The diode reverse recovery current is a problem as a result, the overall efficiency of the converter is increased when operating with high power levels. In [10], a non-isolated dc-dc converter operating with high voltage conversion ratio, as the quadratic boost converter, but additional inductors and filter capacitors must be used and the switch voltage is high. In [11], a new alternative for the implementation of high step-up structures has been presented with the use of the voltage multiplier units integrated with classical non-isolated DC-DC boost converters. This topology solves some of the classical boost converters. However, the power transformer volume is a problem for this topology due to high switching losses and the reduction of overall efficiency. In [12], proposed a new DC-DC converter based on switched capacitor with voltage regulation for PV panels. The most important benefits of the proposed converter are approximately continuous input current, reduction of the number of power components (such as power switches) and overall cost. But the normalized voltage of some power switches is high and the normalized voltage of the output diode nearly to output voltage.

In this study, a new non-isolated DC-DC boost converter based on interleaving technique and switched capacitor is presented. In fact, the proposed converter can be used for different power level by decreasing the nominal value (by increasing the voltage multiplier units between phases) of power components in high voltage gain.

2. Proposed Converter and Principle of Operation

The power circuit of proposed converter is shown in Fig. 1. The proposed converter is a three-phase interleaved high step-up dc/dc converter. The proposed converter consists of the input dc voltage source, voltage multiplier units (consists of three capacitors and 4 diodes), one inductor and one switch for each phase. The phases are connected in parallel to each other. In fact, each phase is a conventional boost dc/dc converter which consists of a power switch, a diode, and one inductor. In addition, by increasing of series the voltage multiplier units, not only increases the voltage gain, but also decreases the normalized voltage stress across semiconductors (by decreasing the nominal value of components).

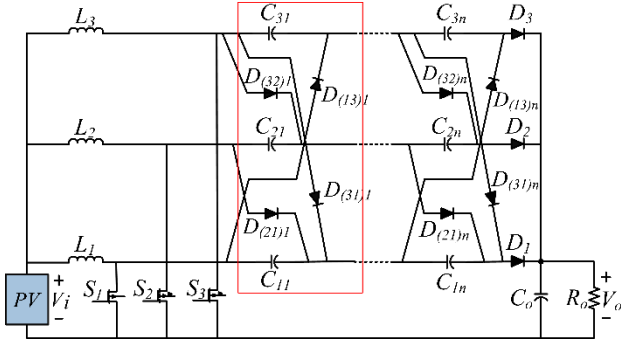


Fig. 1. The power circuit of proposed topology

3. Analysis the Proposed Structure

Theoretical analysis of the proposed operating in CCM (continuous conduction mode) state is provided. In order to simplify the operation analysis of proposed converter, the below assumptions are considered:

- The value of input voltage is constant.
- All used elements are ideal.
- All capacitors are large enough that the voltage of all capacitors considered constant values in one switching period.

For each power switch in one switching period of the proposed converter (T_s) can be considered two- time blank. In the first time blank (DT_s), the power switch is on-state and the second time blank ($(1-D)T_s$), the power switch is off-state.

The Equivalent circuits of the proposed converter at CCM (continuous conduction mode) operation are shown in Fig. 2.

The operation of proposed converter at CCM operation comprises of six modes.

Mode 1 ($t_0=0 \leq t \leq t_1=(D-\frac{1}{3})T_s$): During this mode, the switches S_1 and S_2 are on-state. Also, the diodes D_3 , D_{31} and D_{32} are in forward-bias. In this mode, the current of inductors L_1 and L_2 are linearly increased by the input voltage (V_i) and the current of the inductor L_3 is linearly reduced. In this mode, the voltage of the inductors are:

$$v_{L1} = v_{L2} = V_i \quad (1)$$

$$v_{L3} = V_i + V_{C11} = V_i + V_{C21} \quad (2)$$

The maximum voltage across diodes obtained as follows:

$$v_{D1} = v_{D2} = V_{C31} \quad (3)$$

$$v_{D21} = V_{C11} \quad (4)$$

The maximum voltage across switch S_3 obtained as follows:

$$V_{S3} = -V_{C11} \quad (5)$$

Mode 2 ($t_1=(D-\frac{1}{3})T_s \leq t \leq t_2=\frac{1}{3}T_s$): In this mode, the switch S_1 is on-state. The diodes D_1 , D_{13} and D_{32} are in reversed-bias and the other diodes are in forward-bias. The current of the inductors L_2 and L_3 are linearly reduced and the current of the inductor L_1 is linearly increased by the input voltage (V_i). In this mode, the voltage of the inductors are:

$$v_{L1} = V_i \quad (6)$$

$$v_{L2} = V_i + V_{C11} = V_i - V_o - V_{C21} \quad (7)$$

$$v_{L3} = V_i + V_{C11} \quad (8)$$

In addition, from this mode can be written as follows equation:

$$V_{C21} = V_{C31} \quad (9)$$

The maximum voltage across diode D_{32} obtained as follows:

$$v_{D32} = V_{C31} \quad (10)$$

The maximum voltage across switch S_2 obtained as follows:

$$V_{S2} = -V_{C11} \quad (11)$$

Mode 3 ($t_2=\frac{1}{3}T_s \leq t \leq t_3=DT_s$): During this mode, the switches S_1 and S_3 are on-state. The diodes D_2 and D_{21} are in forward-bias and the other diodes are in reversed-bias. The current of inductors L_1 and L_3 are linearly increased by the input voltage (V_i) and the current of the inductor L_2 is linearly reduced. In this mode, the voltage of the inductors are:

$$v_{L1} = v_{L3} = V_i \quad (12)$$

$$v_{L2} = V_i + V_{C11} \quad (13)$$

The maximum voltage across diodes obtained as follows:

$$v_{D3} = -V_{C31} - V_{C31} \quad (14)$$

$$v_{D31} = V_{C11} \quad (15)$$

$$v_{D13} = V_{C31} \quad (16)$$

Mode 4 ($t_3=DT_s \leq t \leq t_4=\frac{2}{3}T_s$): In this mode, the switch S_3 is on-state. The diodes D_1 , D_2 and D_{13} are in forward-bias and the other diodes are in reversed-bias. The current of the inductors L_1 and L_2 are linearly reduced and the current of the inductor L_3 is linearly increased by the input voltage (V_i). In this mode, the voltage of the inductors are:

$$v_{L1} = V_i + V_{C31} \quad (17)$$

$$v_{L2} = V_i + V_{C11} + V_{31} - V_{C21} \quad (18)$$

$$v_{L3} = V_i \quad (19)$$

The maximum voltage across switch S_1 obtained as follows:

$$V_{S1} = -V_{C31} \quad (20)$$

Mode 5 ($t_4=\frac{2}{3}T_s \leq t \leq t_5=(D+\frac{1}{3})T_s$): During this mode, the switches S_2 and S_3 are on-state. The diodes D_1 and D_{13} are in forward-bias and the other diodes are in reversed-bias. The current of inductors L_2 and L_3 are linearly increased by the input voltage (V_i) and the current of the inductor L_1 is linearly reduced. In this mode, the voltage of the inductors are:

$$v_{L1} = V_i + V_{C31} \quad (21)$$

$$v_{L2} = v_{L3} = V_i \quad (22)$$

Mode 6 ($t_5=(D+\frac{1}{3})T_s \leq t \leq t_6=T_s$): In this mode, the switch S_2 is on-state. The diodes D_1 , D_3 and D_{32} are in forward-bias and the other diodes are in reversed-bias. The current of the inductors L_1 and L_3 are linearly reduced and the current of the inductor L_2 is linearly increased by the input voltage (V_i). In this mode, the voltage of the inductors are:

$$v_{L1} = V_i + V_{C21} + V_{C31} - V_{C11} \quad (23)$$

$$v_{L2} = V_i \quad (24)$$

$$v_{L3} = V_i + V_{C11} \quad (25)$$

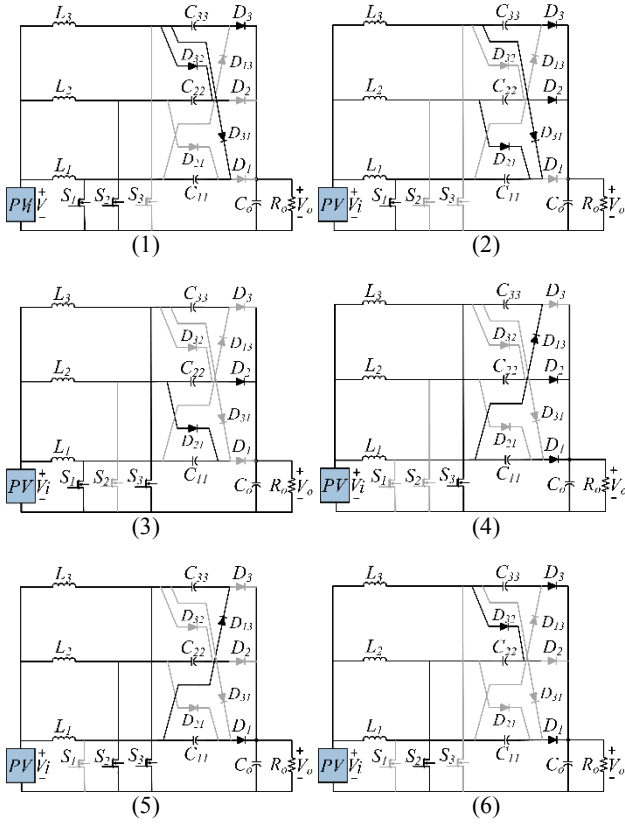


Fig. 2. The equivalent circuits of proposed converter at CCM operation (with $n=1$)

By applying the volt-second balance for the voltage of the inductor, the voltage gain of proposed converter can be obtained as follows equation (for $n=1$):

$$M = \frac{V_o}{V_i} = \frac{2}{1-D} \quad (26)$$

The normalized voltage stress across switches obtained as follows:

$$M_{S1} = M_{S2} = M_{S3} = \frac{1}{2} \quad (27)$$

The normalized voltage stresses across diodes D_1 , D_2 and D_3 can be obtained as follows:

$$M_{D11} = M_{D21} = M_{D31} = 1 \quad (28)$$

Also, the normalized voltage stresses across diodes D_1 , D_2 and D_3 can be obtained as follows:

$$M_{D1} = M_{D2} = M_{D3} = \frac{1}{2} \quad (29)$$

It is clear that the proposed converter has the highest voltage gain when the extended to n stages. The voltage gain of the proposed converter with n stage can be obtained as follows:

$$M = \frac{V_o}{V_i} = \frac{n+1}{1-D} \quad (30)$$

The normalized voltage stress across switches obtained as follows:

$$M_{S1} = M_{S2} = M_{S3} = \frac{1}{n+1} \quad (31)$$

The normalized voltage stresses across diodes D_1 , D_2 and D_3 can be obtained as follows:

$$\begin{cases} M_{D1j} = M_{D2j} = M_{D3j} = \frac{2}{j+1} \\ j = 1, 2, \dots, n \end{cases} \quad (32)$$

Also, the normalized voltage stresses across diodes D_1 , D_2 and D_3 can be obtained as follows:

$$M_{D1} = M_{D2} = M_{D3} = \frac{1}{n+1} \quad (33)$$

The main waveforms of the proposed converter in CCM operation are shown in Fig. 3.

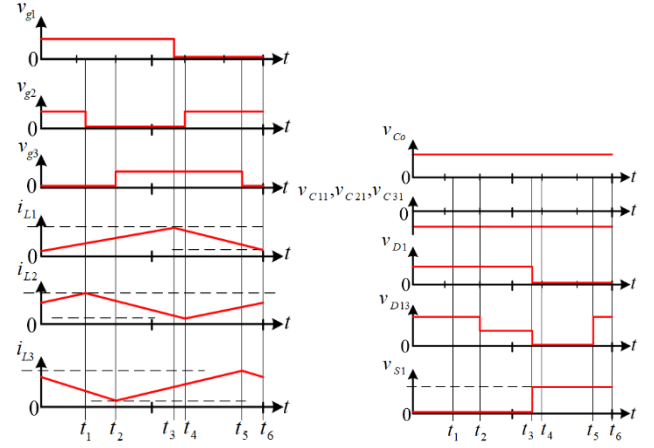


Fig. 3. The main waveforms of proposed converter at CCM operation with $n=1$

5. Comparison Study

In this section, the proposed converter is compared to other topologies. Fig. 4 illustrates a comparison between the proposed converter and the other topologies. Fig. 4(a) illustrates the comparison between the voltage gain (M) of proposed converter versus duty-cycle (D) and other topologies. According to this figure, it is clear that the voltage gain of proposed converter is high than other topologies when the number of n (n =voltage multiplier units) is 2 and greater this. In addition, not only the voltage gain of proposed converter is increased by raising n but also, the stress voltage across switches and diodes will be reduced (by the reduction of nominal values of components). Although the components number of voltage multiplier units will be slightly more in higher stages of n , the proposed converter in high power level has high efficiency. In fact, by decreasing the nominal value of components, the maximum voltage stress of power components will be decreased. Finally, the overall cost of proposed converter will be reduced and efficiency is increased.

Fig. 4(b) illustrates comparison the normalized voltage stress across switches and voltage conversion ratio between the proposed converter and other topologies. From this Fig, it is clear that the normalized voltage across power switches is lower other structure when the number of n is increasing. In the limit, as the number of n gets high in Fig. 4(b), the relationship $\frac{M_{S(\text{switches})}}{M}$ approaches $\frac{1}{n+1}$ for proposed converter that is shown on curves. Therefore, the used power switches for the

proposed converter can be has a low cost, also the overall cost of the proposed converter will be reduced and the efficiency will be increased compared to the other topologies in differences power levels.

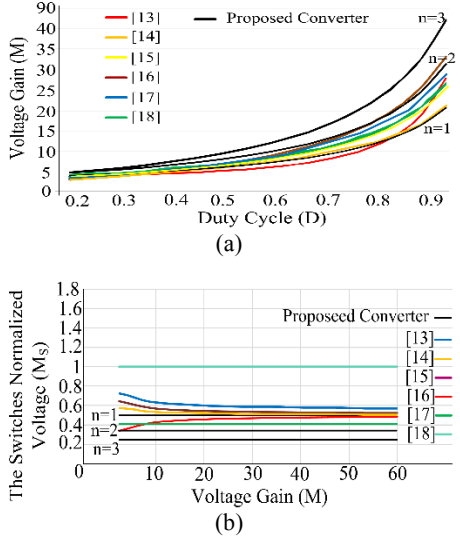


Fig. 4. Comparison the proposed converter with other topologies, (a) the voltage gain versus duty-cycle, (b) the stress voltage across switches versus voltage gain

6. Simulation and Experimental Results

In order to verify the theoretical analysis, the proposed converter is simulated in PSCAD/EMTDC comprehensive and the components specifications of the simulation results are provided in Table 1.

Table 1: The characteristic of the proposed converter

Input voltage	24V
Switching frequency	25kHz
All inductors	1mH
All capacitors of voltage multiplier units	330 μ F
Output capacitor C_o	470 μ F
Output resistance R	100 Ω

Figs. 5- 10 illustrate the simulated waveforms of the proposed converter in CCM operation for $D=0.6$ value (with $n=1$ and $n=2$ stage). Where in this section, all the figures (a) are for $n=1$ stage and figures (b) for the $n=2$ stage. Fig. 5 illustrates the output voltage waveforms of proposed converter. Fig. 5(a) illustrates the output voltage (V_o) with $n=1$ that is about 119.7. Fig. 5(b) illustrates the output voltage (V_o) with $n=2$ that is about 178.8. Fig. 6(a) illustrates the waveform of the inductor L_1 (with 1.95A average value) which the peak to peak current ripple is about 0.56A (the percent current ripple is about 28%). Fig. 6(b) illustrates the waveform of the inductor L_1 (with 5.05A average value) which the peak to peak current ripple is about 0.56A (the percent current ripple is about 11%). Figs. 7(a) and (b) illustrate the capacitor C_{11} voltage which is about 59.8V. Figs. 8(a) and (b) illustrate the voltage across diode D_1 that is about 59.9V and

59.7, respectively (using (33), these values are matched). It is clear that the normalized voltage stress across power diodes is decreased by increasing the number of n . Therefore, at high power levels is not a problem for power diodes. The voltage across the diode D_{21} (shown in Fig. 9) with $n=1$ stage and the $n=2$ stage is nearly 120V (using (32), these values are matched). The maximum voltage across the switch S_1 is about 60V which is shown in Fig. 10 (using (31), these values are matched).

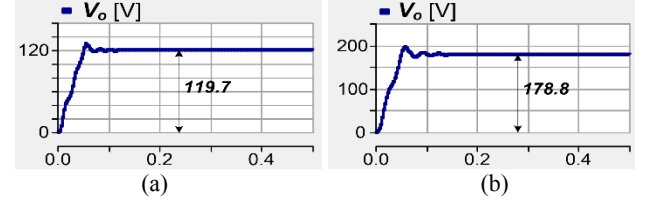


Fig. 5. The equivalent circuits of proposed converter at CCM operation, (a) with $n=1$, (b) with $n=2$

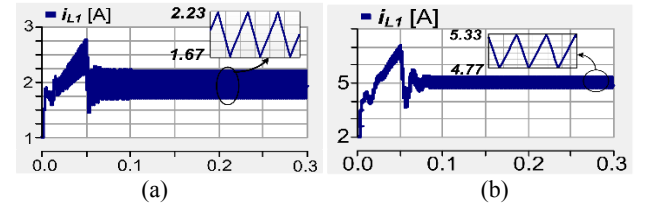


Fig. 6. The equivalent circuits of proposed converter at CCM operation, (a) with $n=1$, (b) with $n=2$

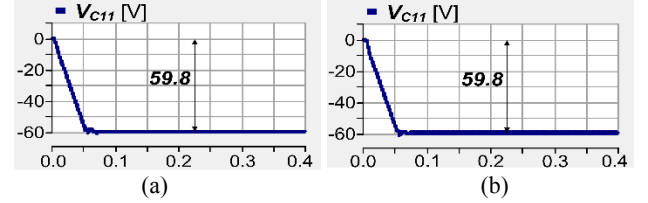


Fig. 7. The equivalent circuits of proposed converter at CCM operation, (a) with $n=1$, (b) with $n=2$

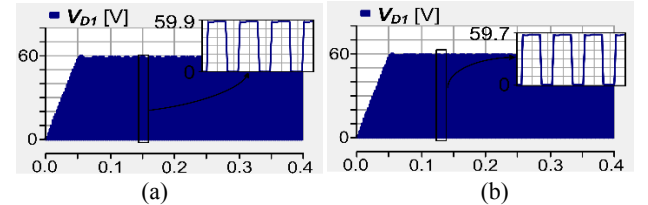


Fig. 8. The equivalent circuits of proposed converter at CCM operation, (a) with $n=1$, (b) with $n=2$

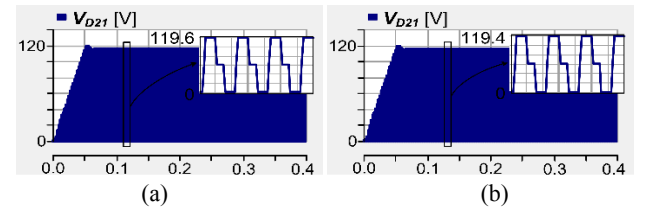


Fig. 9. The equivalent circuits of proposed converter at CCM operation, (a) with $n=1$, (b) with $n=2$

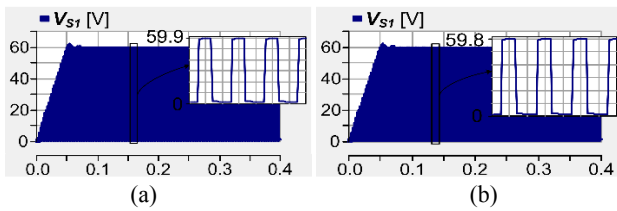


Fig. 10. The equivalent circuits of proposed converter at CCM operation, (a) with $n=1$, (b) with $n=2$

7. Conclusion

In this paper, a new three-phase interleaved high step-up dc-dc converter is presented with reduced voltage stress on semiconductors and higher efficiency about 96.3%. By series increasing number of the voltage multiplier units, the voltage gain of proposed converter is increased and also, the current level is raised. Therefore, the power level of proposed converter is increased. In addition, this leads to reducing the nominal value of power components and normalized voltage stress across switches and diodes. Given these benefits and due to the utilization of interleaving techniques which makes the proposed converter appropriate for renewable energies such as PV applications. The simulation results of proposed converter with 144W and 324W by operating at 25kHz are provided. The simulation results illustrate that the proposed converter achieves the low voltage stress of power switches and diodes, and the efficiency higher than 95.1% in about all power level.

8. References

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