A New Topology for High Step-Up DC-DC Converters

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Abstract

This paper proposes a new topology with high voltage gain and low voltage stress across the devices. The proposed converter combines the conventional boost converter with a switched-inductor branch (SIB) and one inductor-capacitor-diode (*L-C-D*) cell. The SIB is used at the input side which consists of three diodes and two inductors. During magnetization, the two inductors are charged in parallel and discharged in series during demagnetization. At the output side, above-mentioned *L-C-D* cell comprising two capacitors, one inductor, and one diode is used. Therefore, the proposed converter can achieve high voltage gains without extreme duty cycle values. Besides, the normalized devices voltage stress is low which causes the devices nominal voltage to be reduced. The operation principles are explained and the analysis of the devices voltage stress is accomplished. The circuit performance is compared with other solutions in the literature. Eventually, the converter operation is verified using simulation results.

1. Introduction

Nowadays, several applications such as uninterruptible power supplies, electrical vehicles, and distributed generation employ high step-up dc-dc converters [1]. Recently, several types of high step-up dc-dc converters have been presented in the literature. Application of isolated transformer-based dc-dc converters due to the increased size, volume, and weight and low efficiency is limited [2]. Accordingly, transformer less high step-up dc-dc converters are good candidates due to the higher efficiency and lower cost and weight.

Theoretically, the conventional boost converter can provide high voltage gain at duty cycles around unity. However, in practical applications, due to the presence of parasitic components of inductors, capacitors, and semiconductors, the voltage gain in duty cycles around unity is reduced. Moreover, in this converter, the voltage stress of the switch is equal to the output voltage which restricts converter utilization in high output voltages [3, 4]. The voltage gain of cascaded boost converter presented in [5] is high at low values of the duty cycle. Nevertheless, as the number of stages increases, the control complexity is also increased and the voltage stress across the switch is still high [6]. Quadratic boost converter in [7] can alleviate the complex control problem of the cascaded boost converter, however, the voltage stress of the switch is equal to the output voltage and the switch current stress is high [8]. By adjusting the turn's ratio of the coupled inductor and also duty cycle in the coupled-inductor-based converters, high voltage gain is achieved, however, the leakage inductance results in higher voltage stress across the main switches [9]. The combination of the interleaved two boost converter with a voltage multiplier cell composing switched capacitors and coupled inductors, can produce high voltage gain and minimize the input current ripple. However, the cost and control complexity is increased [10, 11]. The voltage gain and efficiency of the double-boost converter in [12] are high. However, this converter requires a large input inductor for reducing the input current ripple which increases the manufacturing cost, circuit size, and overall losses. The voltage gain of CUK-extension converter in [13] is higher than converter in [12] and its semiconductors voltage stress is low. High-voltage inverting Zeta-derived topology in [13] has semiconductors voltage stress which approaches output voltage for high values of the voltage gain. Switched-capacitor-based boost converter in [14] can produce a high voltage gain, however, the semiconductors voltage stress is high. Converter presented in [15] is a high voltage gain converter in which as the voltage gain increases, the voltage stress on switches and diodes approaches to the half of the output voltage.

In this paper, a novel high step-up dc-dc converter combining the conventional boost converter with a switched-inductor branch (SIB) and one inductor-capacitor-diode (*L-C-D*) cell is proposed. The proposed converter possesses the following features: (1) Reduction of voltage stress on power devices. (2) Attaining higher voltage gains with low duty cycles due to the utilization of SIB and *L-C-D* cell. The paper is organized as follows: in section 2, the proposed converter and its detailed analysis are presented. Analysis of the voltage stress of the devices is performed in section 3. A Comparison between the proposed converter and other high step-up topologies in literature is shown in section 4. The simulation results are given in section 5. Section 6 is allocated to the conclusion.

2. Proposed Converter Structure

Fig. 1(a) illustrates the proposed high step-up converter which is constituted three main sections. The first section called SIB comprises two inductors and three diodes. In the middle and last sections, the conventional boost converter is combined with one *L-C-D* cell. This cell consists of one diode, two capacitors, and one inductor. In the proposed topology, the switch S_1 is the main switch and the other (S_2) is used as a synchronous rectifier. The operation principles of the proposed converter are explained in details in the following. To simplify the converter analysis, the following assumptions are considered

- The input voltage source is constant.
- All used devices are considered ideally, therefore the efficiency is 100%.
- The capacitances are high enough that their voltage ripples can be ignored.

2.1. First Operation Mode ($0 \le t < t_1 = DT$)

The equivalent circuit of the first mode is shown in Fig. 1(b). In this mode, the switch S_1 is turned on and the switch S_2 is turned-off. The diodes D_1 and D_2 are directly biased and the diodes D_3 and D_4 are reverse biased. During this mode, the voltage across the inductors L_1 and L_2 is V_i. Accordingly, L_1 and L_2 are magnetized in parallel with the input voltage V_i. In this mode, the current of L_1, L_2, and L_3 is linearly increased. Based on Fig. 1(b), it is clear that capacitor C_2 is charged by capacitor C_1 current. According to Fig. 1(b), we have

$$v_{L1} = v_{L2} = v_L = V_i \quad (1)$$

$$v_{L3} = V_{C1} - V_{C2} \quad (2)$$

$$v_{S2} = V_{C1} \quad (3)$$

$$v_{D3} = -V_i \quad (4)$$

$$v_{D4} = V_{C2} - V_o \quad (5)$$

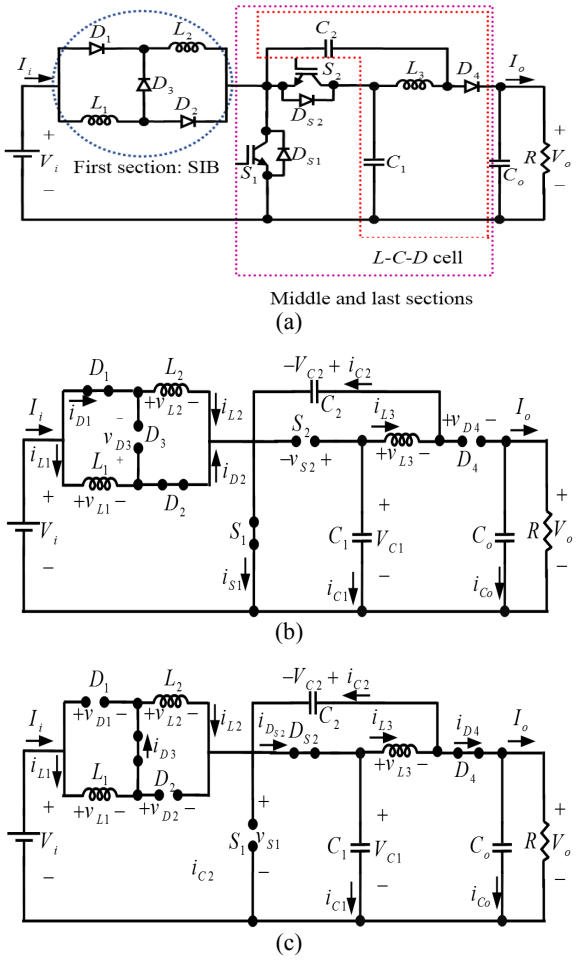


Fig. 1.(a) The structure of proposed high step-up dc-dc converter, **(b)** The equivalent circuit in the first operation mode, **(c)** The equivalent circuit in the second operation mode

2.2. Second Operation Mode ($t_1 = DT \le t < T$)

Fig. 1(c) illustrates the equivalent circuit of proposed converter in the second operation mode. At time t_1 the switch S_1 is turned off and the switch S_2 is turned on. Moreover, the diodes D_3 and D_4 are directly biased and create a path for inductors current. The diodes D_1 and D_2 are reverse biased. During this mode, the inductors L_1, L_2, and L_3 current are linearly reduced. The capacitors C_1 and C_o are charged by the currents i_{DS2}-i_{L3} and i_{D4}, respectively. Then, the below equations can be written

$$V_o = V_{C1} + V_{C2} \quad (6)$$

$$2v_L + V_{C1} = V_i \quad (7)$$

$$v_{D1} = v_{D2} = v_L \quad (8)$$

$$v_{L3} = -V_{C2} = V_{C1} - V_o \quad (9)$$

$$v_{S1} = V_{C1} \quad (10)$$

According to (7), following equation can be written in the second operation mode

$$v_{L1} = v_{L2} = v_L = \frac{V_i - V_{C1}}{2} \quad (11)$$

By applying volt-second balance for the inductors L_1, L_2, and L_3, the voltage of capacitors will be

$$V_{C1} = \frac{V_{C2}}{D} = \frac{1+D}{1-D} V_i \quad (12)$$

By combining (6) and (12), the voltage gain of proposed converter (M) is obtained as follows

$$M = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{(1+D)^2}{1-D} \quad (13)$$

Fig. 2(a) demonstrates the key waveforms of proposed converter.

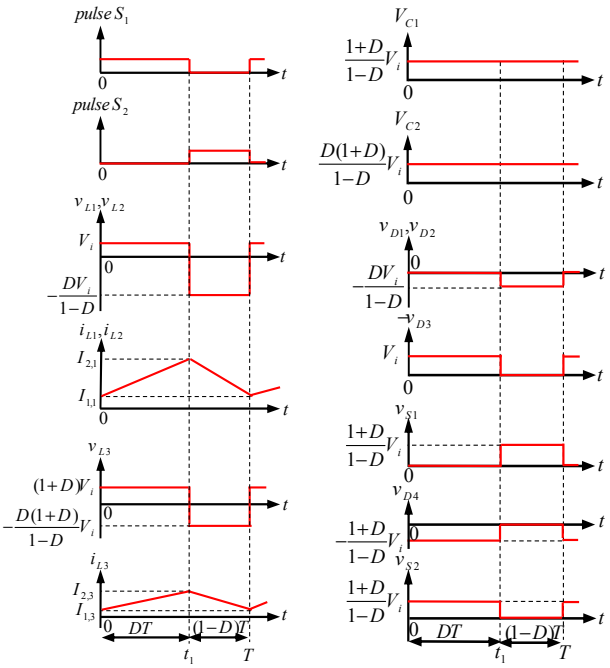


Fig. 2. Key waveforms of the proposed converter

3. Voltage Stress Analysis

In this section, devices voltage stress are calculated. Voltages are normalized with respect to the output voltage (V_o). From Eq. (13), the following expression can be written

$$D = \frac{-(M+2)+\sqrt{M^2+8M}}{2} \tag{14}$$

3.1. Normalized Voltage Stress across Switches

Using (3), (10), (12) and (14), the normalized switches S_1 and S_2 voltage stress (M_{S1} and M_{S2}) is equal to

$$M_{S1,2} = \frac{v_{S1}}{V_o} = \frac{V_{C1}}{V_o} = \frac{2}{\sqrt{M^2+8M}-M} \tag{15}$$

3.2. Normalized Voltage Stress across Diodes

Referring to Fig. 2, it is clear that the diodes D_1 and D_2 maximum voltage is equal to each other. Hence, using (8), (11), (12) and (14) the following equation is obtained

$$M_{D1,2} = \frac{\sqrt{M^2+8M}-(M+2)}{M^2+M\,(4-\sqrt{M^2+8M}\,)} \tag{16}$$

According to Fig. 2, the normalized voltage stress of diode D_3 is equal to

$$M_{D3} = \frac{v_{D3}}{V_o} = \frac{1}{M} \tag{17}$$

From Fig. 2 and using (5), (12), (13) and (14) the following equation is obtained for normalized voltage stress of diode D_4

$$M_{D4} = \frac{v_{D4}}{V_o} = \frac{2}{\sqrt{M^2+8M}-M} \tag{18}$$

3.3. Normalized Voltage Stress across Capacitors

By the use of (12) and (14), the normalized voltage stress of capacitors C_1 and C_2 is obtained

$$M_{C1} = \frac{V_{C1}}{V_o} = \frac{2}{\sqrt{M^2+8M}-M} \tag{19}$$

$$M_{C2} = \frac{V_{C2}}{V_o} = \frac{\sqrt{M^2+8M}-(M+2)}{\sqrt{M^2+8M}-M} \tag{20}$$

From Fig. 1(a), it is obvious that the voltage across the output capacitor is always equal to V_o. Therefore, the normalized voltage stress across the capacitor C_o is given by

$$M_{Co} = \frac{V_{Co}}{V_o} = \frac{V_o}{V_o} = 1 \tag{21}$$

Table 1 shows the devices normalized peak voltage stress. Fig. 3 demonstrates the capacitors voltage stress. As shown in Fig. 3, the voltage stress on entire capacitors except C_o is less than the output voltage. For capacitor C_o, regardless of the voltage gain, the normalized voltage stress is constant. For capacitors C_1 and C_2, as the voltage gain is increased, the normalized voltage stress approaches to 0.5. Accordingly, in the proposed converter, the voltage stress across the capacitors is low which makes possible the use of low nominal voltage capacitors.

Table 1. Devices voltage and current stress

Device	Normalized peak voltage
S_1 and S_2	$\frac{2}{\sqrt{M^2+8M}-M}$
D_1 and D_2	$\frac{\sqrt{M^2+8M}-(M+2)}{M^2+M\,(4-\sqrt{M^2+8M}\,)}$
D_3	$\frac{1}{M}$
D_4	$\frac{2}{\sqrt{M^2+8M}-M}$
C_1	$\frac{2}{\sqrt{M^2+8M}-M}$
C_2	$\frac{\sqrt{M^2+8M}-(M+2)}{\sqrt{M^2+8M}-M}$
C_o	1

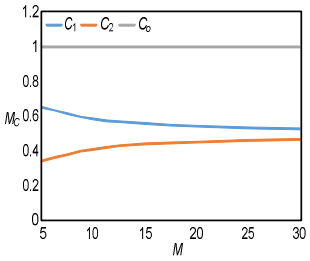


Fig. 3. The normalized voltage stress of the capacitors

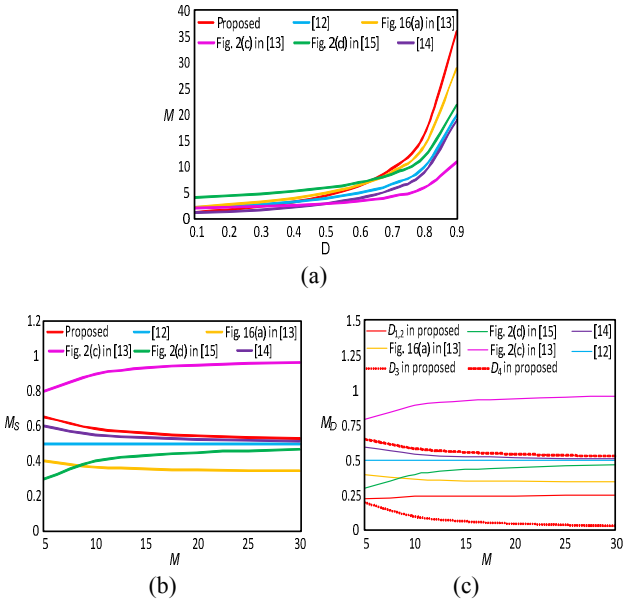
4. Comparison Study

In this section, a comparison is accomplished between proposed high step-up converter and other high step-up converters in literature, in terms of voltage gain and normalized voltage stress across power switch and diodes. The results of the comparison are tabulated in Table 2 and are plotted in Fig. 4. Fig. 4(a) illustrates a comparison between the voltage gain of proposed converter and other high step-up converters. As can be seen, for D<0.64, the converter of Fig. 2(d) in [15] has higher voltage gain compared to other step-up converters in literature. For D>0.64, the proposed converter has highest voltage gain. Moreover, for a same value of the voltage gain, the proposed structure operates at smaller values of the duty cycle which simplify the converter controllability and increases its stability. Fig. 4(b) demonstrates a comparison between normalized switch voltage stress of the proposed converter and five other topologies with respect to M. According to this figure, for small values of M, converters of [12], Fig. 16(a) in [13], [14], and Fig. 2(d) in [15] have lower normalized switch voltage stress in comparison with the proposed converter. However, as the voltage gain increases, M_S of proposed topology and converters of [12], [14], and Fig. 2(d) in [15] all approaches to 0.5. To

compare the normalized voltage stress of the diodes between the proposed converter and five other circuits graphically, Fig. 4(c) is depicted. According to Fig. 4(c), the diodes D_1, D_2, and D_3 of proposed converter have lower normalized voltage stress compared to other structures. Converters in [12] and [14] and converters of Fig. 16(a) in [13] and Fig. 2(d) in [15] have lower normalized diode voltage stress than diode D_4 in proposed converter. Besides, as the M increase, the normalized voltage stress of diodes $D_{1,2}$, D_3, and D_4 in proposed converter approaches to 0.25, 0, and 0.5, respectively.

Table 2. Comparison between proposed converter and other high step-up topologies

Topology	M	M_S	M_D
Proposed	$\frac{(1+D)^2}{1-D}$	$\frac{2}{\sqrt{M^2+8M}-M}$	$M_{D1,2}=\frac{\sqrt{M^2+8M}-(M+2)}{M^2+M(4-\sqrt{M^2+8M})}$, $M_{D3}=\frac{1}{M}$, $M_{D4}=\frac{2}{\sqrt{M^2+8M}-M}$
[12]	$\frac{2}{1-D}$	0.5	0.5
Fig. 2(c) in [13]	$\frac{2-D}{1-D}$	$\frac{M-1}{M}$	$\frac{M-1}{M}$
Fig. 16(a) in [13]	$\frac{2+D}{1-D}$	$\frac{1+M}{3M}$	$\frac{1+M}{3M}$
[14]	$\frac{1+D}{1-D}$	$\frac{M+1}{2M}$	$\frac{M+1}{2M}$
Fig. 2(d) in [15]	$\frac{4-2D}{1-D}$	$\frac{M-2}{2M}$	$\frac{M-2}{2M}$



(a) (b) (c)

Fig. 4. Comparison of the proposed converter and other high step-up topologies, **(a)** The voltage gain comparison, **(b)** The normalized switch voltage stress comparison, **(c)** The normalized diodes voltage stress comparison

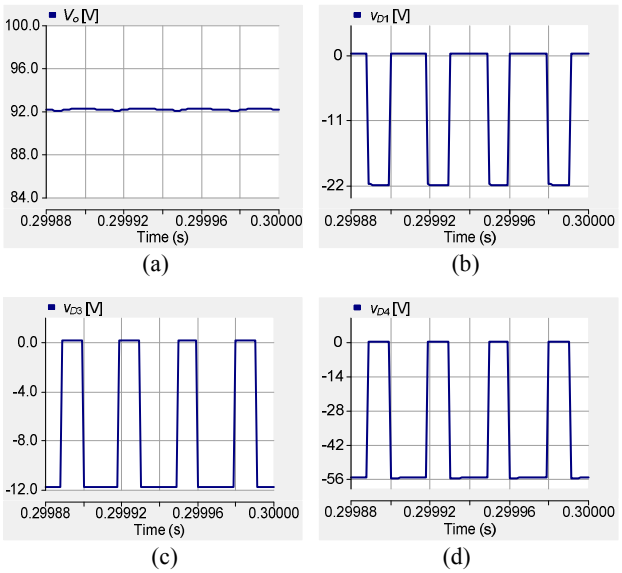
5. Simulation Results

In order to verify the theoretical analysis, the proposed converter of Fig. 1(a) is simulated by PSCAD/EMTDC software. The device's specifications of proposed converter are tabulated in Table 3. The simulation waveforms of proposed structure are shown in Figs. 5-7.

Table 3. The characteristics of proposed converter

	Parameter	Value
Converter	Input Voltage (V_i)	12 V
	Duty Cycle of the Switch (D)	0.65
	C_1, C_2, and C_o Capacitors	100 µF
	L_1-L_3 Inductors	1 mH
	Switching Frequency (f)	33 kHz

The waveforms of the output voltage, diodes D_1, D_3, and D_4 voltage are shown in Fig. 5. The waveform of diode D_2 voltage is not shown because it is similar to diode D_1 voltage waveform. It is obvious from Fig. 5(a) that the value of output voltage is almost 92 V. As shown in Fig. 5(b), (c), and (d), the voltage stress across diodes D_1, D_3, and D_4 are less than the output voltage and almost 22 V, 12 V, and 56 V, respectively. Thus, their normalized voltage stress is almost 23.91%, 13.04%, and 60.87%, respectively. According to Fig 6(a) and (b), the voltage stress of switches is about 56 V. Therefore, the normalized switches voltage stress is about 60.87%. The voltage waveforms of capacitors C_1 and C_2 are shown in Fig. 6(c) and (d), respectively. As shown in Fig. 6(c), the voltage across the capacitor C_1 is nearly 56 V which is in good agreement with the result obtained in Eq. (12). Fig. 6(d) shows that the capacitor C_2 voltage is nearly 36 V. This value conforms to theoretical result. The current waveform of the inductor L_1 is shown in Fig. 7(a). As shown in this figure, the average current of this inductor is about 5 A and its peak to peak ripple is almost 0.25 A. Thus, its percentage of current ripple is 5%. Fig. 7(b) shows that the output current is 1.05 A. Thus, the output power is about 96 W.



(a) (b) (c) (d)

Fig 5. Simulation results of the proposed converter, **(a)** Output voltage (V_o), **(b)** Diode D_1 voltage (v_{D1}), **(c)** Diode D_3 voltage (v_{D3}), **(d)** Diode D_4 voltage (v_{D4})

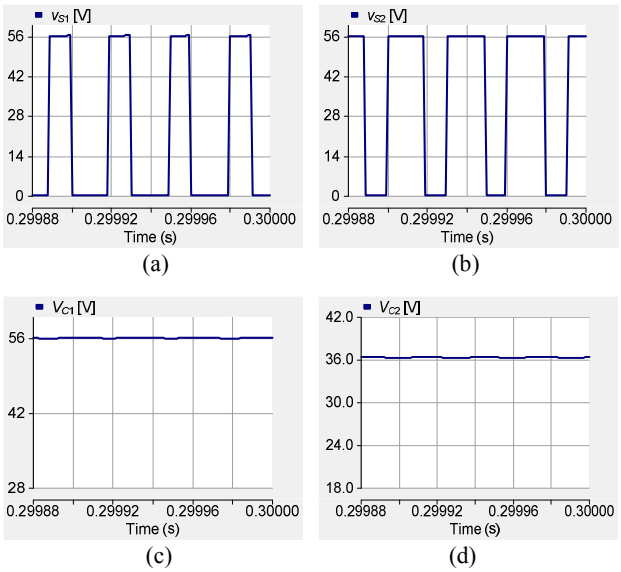


Fig 6. Simulation results of the proposed converter, **(a)** Switch S_1 voltage (v_{S1}), **(b)** Switch S_2 voltage (v_{S2}), **(c)** Capacitor C_1 voltage (V_{C1}), **(d)** Capacitor C_2 voltage (V_{C2})

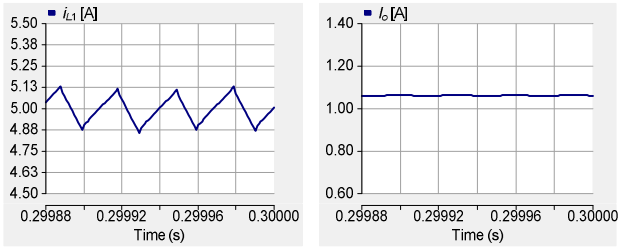


Fig 7. Simulation results of the proposed converter, **(a)** Inductor L_1 current (i_{L1}), **(b)** Output current (I_o)

6. Conclusions

In this paper, a non-isolated dc-dc converter with high voltage gain and low voltage stress across the devices is proposed. The proposed topology comprises one SIB and combination of the conventional boost converter with one *L-C-D* cell. The analysis of the voltage stress of the devices is accomplished. The circuit performance is compared with other step-up structures in the literature in terms of voltage gain and normalized switch and diodes voltage stress. For D>0.64, the proposed converter has much higher voltage gain compared to other converters in literature. As the voltage gain increases, M_S approaches to 0.5 and $M_{D1,2}$, M_{D3}, and M_{D4} approaches to 0.25, 0, 0.5, respectively. Finally, the simulation results confirm the validity of the theoretical analysis.

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