A Novel Hybrid Multiphase Multilevel Inverter Topology

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Abstract

This paper presents a new hybrid multiphase multilevel inverter topology for multiphase systems especially for multiphase machines. The proposed topology is able to generate different voltage levels with less number of power electronic counts. The proposed topology uses unidirectional and bidirectional switches to generate different voltage levels. The common voltage of the proposed topology is zero due to clamping the midpoint of the dc-link multilevel inverter to the ground by bidirectional switches. Fundamental frequency switching is used for triggering the power switches and the results are verified by MATLAB/Simulink software.

Keywords—multiphase multilevel inverter; topology; hybrid topology; multiphase converter

1. Introduction

In recent years, multiphase machines with more than three phases have attracted considerable interest among researchers due to their substantial features. There are many advantages which distinct the multiphase machines in comparison with other three phase machines. As reported in [1], splitting the system power to more than three phases which diminishes the rating of semiconductor devises of the converter is one of the most important multiphase machines' features in contrast with three phase machines. Improving fault tolerance capability without additional hardware requirements, increasing the efficiency, reduction in torque pulsation, high power density and reduced toque ripple are other benefits of the multiphase machines [2-6].

By now, different multilevel inverter topologies are reported in literatures. The most famous topology that is considered a lot due to its modularity is cascaded H-bridge multilevel (CHB) inverter. Requiring isolated dc voltages makes this topology more costly and unreliable. In [7] a five-level five-phase CHB inverter has been presented with a new hybrid modulation technique. Using isolated dc voltage sources makes difficulties for application of this topology.

In this paper, a new multiphase multilevel inverter has been proposed. The proposed inverter employs less umber of power electronic counts in comparison with other topologies. So far, various switching techniques are introduced by researchers such as phase shift Sinusoidal Pulse Width Modulation (SPWM), level shift SPWM, space vector modulation, hybrid modulation, fundamental frequency modulation and so on [7-10]. One of the most important features of the proposed structure is employing simple switching technique for triggering power switches. For the proposed topology, fundamental frequency switching has been used.

This paper is organized as follows. The proposed structure and its operation analysis with control strategy are brought in section II. The comparisons are illustrated in Section III. Simulation results are presented in Section IV and the concluding statements are given in section V.

2. The proposed multiphase multilevel inverter

Fig. 1 illustrates the proposed multiphase multilevel inverter topology. The proposed topology consists of three parts which are named as upper unit, lower unit and auxiliary unit. The upper and lower units which use only unidirectional switches are employed for generating positive and negative voltage levels, respectively. These upper and lower units can be duplicated to generate high voltage levels. The auxiliary unit uses the mixed of unidirectional and bidirectional switches to help for generating voltage levels especially zero level. Clamping the midpoint of the dc-link to the ground causes the common voltage of the inverter becomes zero.

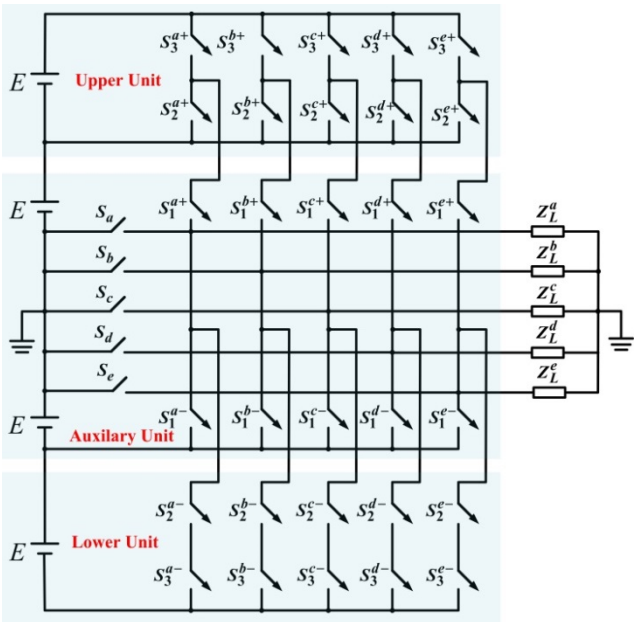

Fig. 1. The proposed multiphase multilevel inverter.

Table 1 illustrates the switching states for the proposed multilevel multiphase inverter of Fig. 1. The switching states have written for phase a. It is important to note that the other phase are similar to phase a with phase difference $\frac{2\pi}{m}$ where m is the number of phases.

Table 1. The switching states of the proposed multiphase multilevel inverter

$V_{Z_L^a}$	S_1^a+	S_2^a+	S_3^a+	S_1^a-	S_2^a-	S_3^a-	S_a
0	off	off	off	off	off	off	on
E	on	on	off	off	off	off	off
2E	on	off	on	off	off	off	off
-E	off	off	off	on	off	off	off
-2E	off	off	off	off	on	on	off

By duplicating the upper and lower units, it is possible that the number of voltage levels increased. According to the above explanations, the number of power switches versus the number of voltage levels for one phase can be calculated as follows:

$$N_{IGBT} = 2\left(N_{level} - 1\right) \tag{1}$$

For m number of phases, the number of power switches is determined by the following term:

$$N_{IGBT} = 2m\left(N_{level} - 1\right) \tag{2}$$

In power electronic converters, each bidirectional and unidirectional switches uses one driver circuit, therefore, the number of driver circuits versus the number of voltage levels are obtained by:

$$N_{IGBT} = 2N_{level} - 3 \tag{3}$$

Similar to way of calculating for power switches, the number of driver circuits for m number of phases is calculated as follows:

$$N_{IGBT} = m\left(2N_{level} - 3\right) \tag{4}$$

It is clear that the power electronic components such as clamping diodes, balancing capacitors, switches and dc bus capacitors are reduced in the proposed switched-capacitors multilevel inverter topology significantly. Fewer number of the power electronic switches leads to the reduction of cost and simple control strategy.

3. Switching technique

For multiphase multilevel inverters, different switching methods have been introduced. Between the switching methods, the fundamental frequency switching is considered due to its simplicity and low frequency switching. One of the most important indexes in inverter's performance is total harmonic distortion (THD) [10], which given by:

$$THD = \frac{\sqrt{\sum_{m=3,5,\ldots}^{\infty} V_{o,m}}}{V_{o,1}} = \sqrt{\left(\frac{V_{o,rms}}{V_{o,1}}\right)^2 - 1} \tag{1}$$

where $V_{o,m}$ is the rms of the m order component of the output voltage. $V_{o,rms}$ and $V_{o,1}$ being the rms values of the output voltage and the fundamental of the output voltage, respectively. The amount of $V_{o,rms}$ and $V_{o,1}$ are computed using the following equation, respectively.

$$V_{o,rms} = \frac{2\sqrt{2}V_b}{\pi}\sqrt{\sum_{m=1}^{\infty}\left(\sum_{i=1}^{N_{level}} \frac{cos(m\theta_i)}{m}\right)^2} \tag{5}$$

$$V_{o,1} = \frac{2\sqrt{2}V_b}{\pi}\sum_{i=1}^{N_{level}} cos\left(m\theta_i\right) \tag{6}$$

where the parameters $\theta_1, \theta_2, \ldots, \theta_{N_{level}}$ are switching angles and given by the following equation:

$$\theta_i = sin^{-1}\left(\frac{i-0.5}{N_{level}}\right), \quad i = 1, 2, \ldots, N_{level} \tag{7}$$

4. Simulation results

In order to validate the proposed topology, computer simulation using MATLAB-Simulink has been created. The simulation parameters have been listed in table 2. Fig. 2 illustrates the proposed 5-phase 7-level inverter for simulations.

Switching table for triggering power switches of the proposed 5-phase 7-level inverter is indicated in table 3. This table has been written for phase a. The other phases i.e. b, c, d and e have $\frac{2\pi}{5}$ phase differences from phase a.

Table 2. The used parameters in simulation for testing

Parameters	**Value**
Input voltages	75 V
Output frequency	50 Hz
Resistive load	50 Ω
Inductive load	80 mH

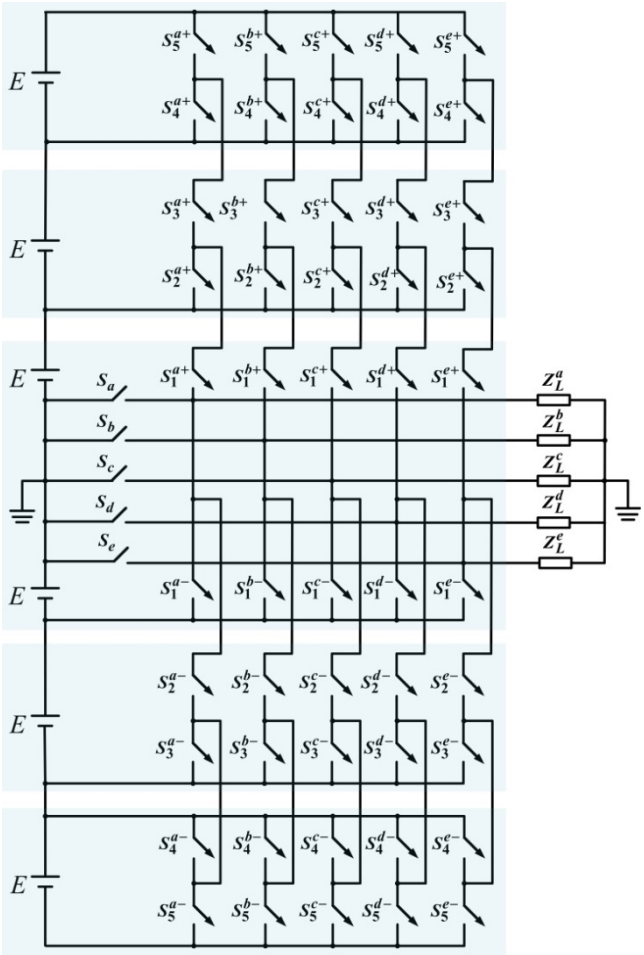

Fig. 2. The proposed 5-phase 7-level inverter.

Table 3. The switching states of the proposed 5-phase 7-level inverter

$V_{Z_L^a}$ / Switches States	0	+E	+2E	+3E	-E	-2E	-3E
S_a	on	off	off	off	off	off	off
S_1^{a+}	off	on	on	on	off	off	off
S_2^{a+}	off	on	off	off	off	off	off
S_3^{a+}	off	off	on	on	off	off	off
S_4^{a+}	off	off	on	off	off	off	off
S_5^{a+}	off	off	off	on	off	off	off
S_1^{a-}	off	off	off	off	on	off	off
S_2^{a-}	off	off	off	off	off	on	on
S_3^{a-}	off	off	off	off	off	on	off
S_4^{a-}	off	off	off	off	off	off	on
S_5^{a-}	off	off	off	off	off	off	off

Figs. 3 and 4 illustrate the output voltage waveforms of the simulated five phase seven level inverter. The waveforms of the phases a to d have 72 degree phase difference with each other as shown in Fig. 3.

Based on FFT analysis the load voltage and current's THD are 11.91%.

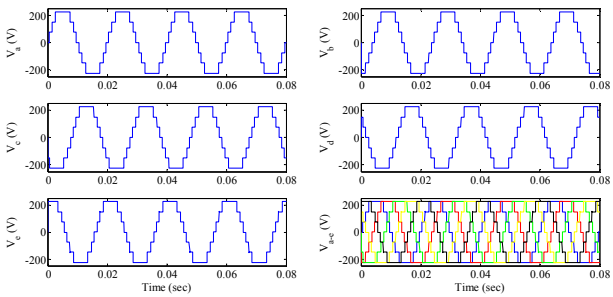

Fig. 3. Output voltage waveforms of the proposed 5-phse 7-level inverter

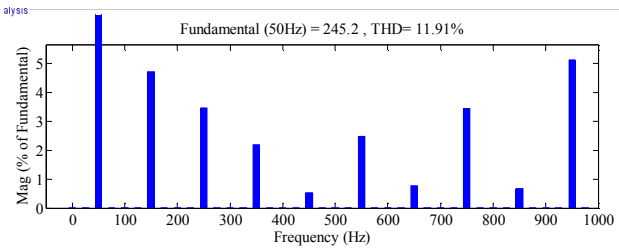

Fig. 4. FFT analysis of the load voltage for the proposed 5-phse 7-level inverter ($THD = 11.91\%$)

Figs. 5 and 6 represent the load current waveforms and its FFT analysis. The FFT analysis shows that the THD of the load current is 3.48%. AS can be seen from the figures, the load current is almost sinusoidal because the load is resistive inductive and acts as a low pass filter for current.

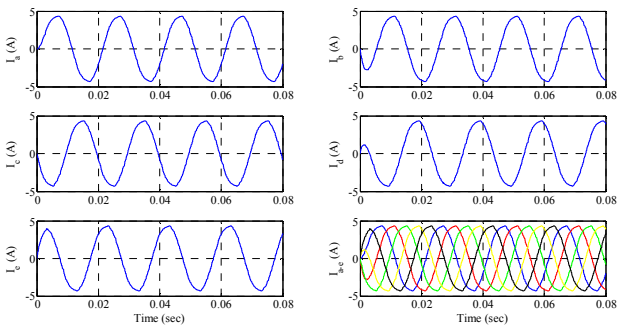

Fig. 5. Output current waveforms of the proposed 5-phse 7-level inverter

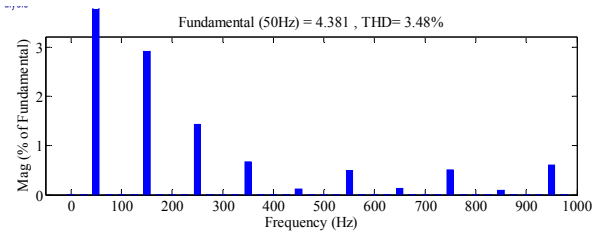

Fig. 6. FFT analysis of the load current for the proposed 5-phse 7-level inverter ($THD_I = 3.48\%$)

5. Conclusions

In this paper, a new multiphase multilevel inverter configuration presented. Generating different multilevel voltages was one of the most important benefits of the proposed structure. The suggested structure employed less number of power electronic counts which reduces the cost of the topology. The proposed structure was able to generate high number of voltage levels in comparison with other multiphase topologies. The simulation results showed that the THD of load voltage and current were 11.91% and 3.48% which could be decreased by increasing the voltage levels. For the future work, the authors apply the suggested topology for a multiphase machine and the closed loop control of the inverter is investigated.

7. References

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