A New Multiport Non-Isolated Bidirectional dc/dc Converter with Zero Voltage Switching and Free Ripple Input Currents

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Abstract

In this paper, a multi-port non-isolated bidirectional dc-dc converter is proposed. Some privileges of the proposed converter are included the capability of zero voltage switching for main switches, capability of zero current switching for the auxiliary switches, cancelling input currents ripple and bidirectional power flow between the ports. By using an inverse coupled inductor and a capacitor the input currents ripple at low voltage side are reduced. In order to achieve zero voltage switching of the main switches in each stages, an auxiliary circuit which is consists of an auxiliary inductor, two switches and two diodes is utilized. In this paper, theoretical analysis for all operating modes of the converter, voltage conversion ratio, required conditions for attaining ZVS operation of switches, voltage and current stresses of all switches, also, the required condition for cancelling input currents ripple in both boost and buck operations are presented. Finally, to testify the validity of theoretical results and demonstrate the performance of the converter, simulation results of the proposed converter in EMTDC/PSCAD software are presented.

1. Introduction

DC-DC converters with soft switching and bidirectional capabilities are more interested to be used in energy conversion applications in renewable energy systems such as fuel cells [1]. In addition, a fuel cell system requires an extra battery to charge for load leveling, also, it should have the ability to discharge at high and low load conditions to have a good performance at transient conditions [2-3]. There are several related converters have been introduced in recent years. In [2-3], converters with three ports are presented. The switches of these converters operate under hard switching condition. Free ripple input current at low voltage side of bidirectional converters is important to achieve. Also, decreasing the voltage ripple at low voltage side would increase the life time of the used battery which is almost placed at low voltage side [4]. The presented bidirectional converter in [4] has the capability of achieving zero voltage switching (ZVS) and suppressing input current ripple at low voltage side. Furthermore, this converter is a kind of two port converter.

An isolated multi-port converter with soft switching operation suitable for fuel cell applications is presented in [5]. However, the losses of the presented converter in [5] is considerable. The conduction loss in isolated bidirectional converters is higher than the non-isolated bidirectional converters [6-7]. Some multiport converters through parallel connecting of bidirectional converters are presented in [8]. Converters which are able to eliminate the input current ripple properly are more acceptable in photovoltaic (PV) applications. In interleaved step-up boost converters, the input current ripple is decreased and they can provide zero input current ripple for a small range of duty cycles [9-12]. The presented boost converters in [9-12] can transfer the power only in one direction. Moreover, in these converters, by using coupled inductors, the voltage gain is increased, also, they are kind of two port converters. In [13-14], several techniques are presented to obtain zero ripples at output voltage in buck and buck-boost dc-dc converters. However, the switches of these topologies operate with hard switching.

In this paper, a new multiport non-isolated bidirectional dc-dc converter with capability of zero voltage switching and free ripple input currents is proposed. The proposed converter is analyzed during a switching period for boost and buck operations of each stages and the voltage gain, voltage and current stress on switches, required ZVS conditions of main switches, required conditions for eliminating input currents ripple are calculated. Finally, to reconfirm the obtained analytical results the EMTDC/PSCAD simulation results are extracted.

2. Proposed Converter

The circuit diagram of the proposed three port non-isolated bidirectional converter is shown in Fig. 1. The proposed converter contains three capacitors of C_{31}, C_{32} and C_4, two inversed coupled inductors, two auxiliary inductors of L_{s1} and L_{s2}, four main switches of S_{11}, S_{12}, S_{21} and S_{22}, four auxiliary switches of S_{31}, S_{32}, S_{41} and S_{42}, the switches' internal diodes D_{11}, D_{12}, D_{21}, D_{22}, D_{31}, D_{32}, D_{41} and D_{42}, blocking diodes of D_{51}, D_{52}, D_{61} and D_{62}, clamping diodes of D_{71}, D_{72}, D_{81} and D_{82}. The coupled inductors are modeled with magnetizing inductance of L_{m1} and L_{m2}, leakage inductance of L_{k1} and L_{k2}, and transformers of T_1 and T_2 with turns ratios of $1:n_1$ and $1:n_2$, respectively. By considering that the capacitors C_{31}, C_{32} and C_4 are large enough the voltages across them can be considered constant as $V_{\ell 1}$, $V_{\ell 2}$ and V_{C4}, respectively. The proposed converter by parallel connecting of several bidirectional stages can be extended to N port converter.

2.1. Boost operating mode

The voltage and current waveforms of the proposed converter in boost operation for $n_j = 1$ (required condition for achieving free ripple input currents) are shown in Fig. 2. The equivalent circuits of the proposed converter for one stage during a switching period are shown in Fig. 3. In the obtained equations the index j shows the value of parameters in stage

j . Where, j is the number of stages (input voltage sources at low voltage side) that is defined as $j = 1,2,....,N$.

2.1.1. First Operating Mode ($t_0 \le t < t_1$):

The equivalent circuit of the first mode for one stage is

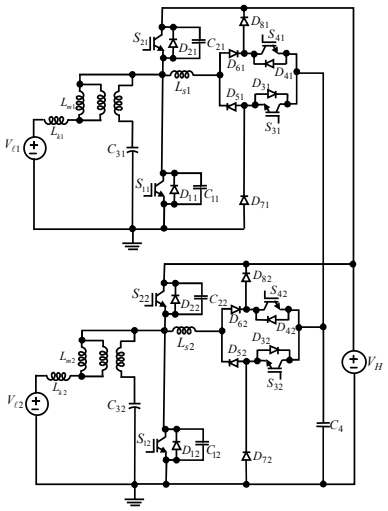


Fig. 1. The power circuit of the proposed three port converter.

shown in Fig. 3(a). In this mode, the internal capacitor of switch C_{2j} is charged and the internal capacitor of switch C_{1j} is discharged. As the time interval of this mode is very short, it is possible to consider the currents i_{Lsj} , i_{Lmj} and i_{Lkj} equal to their initial values of $-I_{s2j}$, I_{m2j} and I_{k2j} , respectively. In this mode, the voltage across the capacitor C_{1j} should be discharged completely to the zero. As a result, the diode of D_{1j} can be turned that it leads to the switch S_1 turn on at ZVS state at second mode. As a result, the time interval of the first mode (T_{1j}) is obtained as following equation:

$$T_{1j} = \frac{n_j(C_{1j} + C_{2j})V_H}{n_j I_{s2j} - (n_j - 1)I_{k2j} - I_{m2j}} \tag{1}$$

2.1.2. Second Operating Mode ($t_1 \le t < t_2$):

The equivalent circuit of second mode for one stage is shown in Fig. 3(b). As mentioned before, this mode starts with ZVS turning on of the switch S_{1j} . In this mode, the voltages across the inductors L_{mj} , L_{kj} and L_{sj} are equal to $V_{\ell j} / n_j$, $(n_j - 1)V_{\ell j}$ and V_{C4} , respectively. As a result, the inductors' currents can be written as follows:

$$i_{Lmj} = \frac{V_{\ell j}}{n_j L_{mj}}(t - t_1) + I_{m2j} \tag{2}$$

$$i_{Lkj} = \frac{(n_j - 1)V_{\ell j}}{n_j L_{kj}}(t - t_1) + I_{k2j} \tag{3}$$

$$i_{Lsj} = -I_{s2j} + \frac{V_{C4}}{L_{sj}}(t - t_1) \tag{4}$$

In this mode, the current i_{S1} is obtained as follows:

$$i_{S1} = \left[\frac{(n_j - 1)^2}{n_j^{\,2}}\frac{V_{\ell j}}{L_{kj}} + \frac{V_{\ell j}}{n^2 L_{mj}} + \frac{V_{C4}}{L_{sj}}\right](t - t_1) + \frac{(n_j - 1)}{n_j}I_{k2j} - I_{s2j} + \frac{I_{m2j}}{n_j} \tag{5}$$

2.1.3. Third Operating Mode ($t_2 \le t < t_3$):

The equivalent circuit third mode for one stage is shown in Fig. 3(c). The current i_{Lsj} and voltage v_{Lsj} reach to zero and the switch S_4 is turned off at ZCS state.

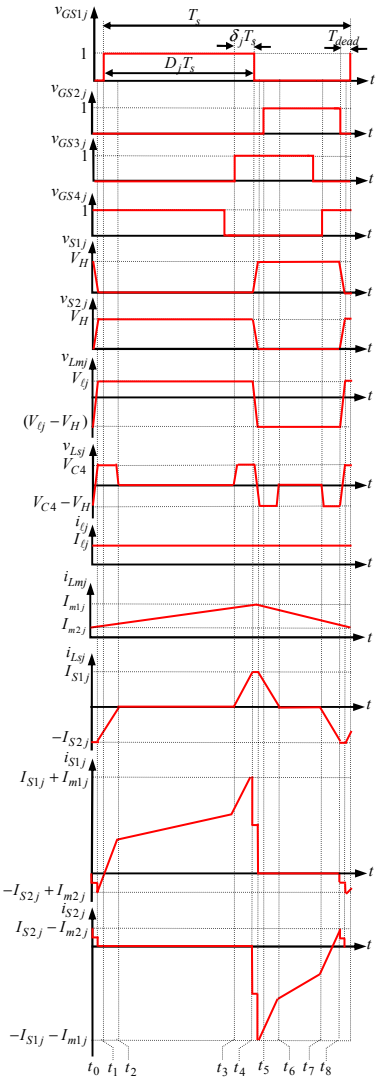


Fig. 2. The waveforms of one stage in the proposed converter for boost operation.

2.1.4. Fourth Operating Mode ($t_3 \le t < t_4$):

The equivalent circuit of fourth mode for one stage is shown in Fig. 3(d). The voltage v_{Lsj} is equal to V_{C4} . As a result, it can be written that:

$$i_{Lsj} = \frac{V_{C4}}{L_{sj}}(t - t_3) \tag{6}$$

Considering Fig. 2, (2) and (4) it can be written that:

$$I_{m1j} = I_{m2j} + \frac{V_{\ell j}}{n_j L_{mj}} D_j T_s \tag{7}$$

$$I_{s1j} = \frac{V_{C4}}{L_{sj}}\delta T_{sj} \tag{8}$$

Where, D is the duty cycle and δT_{sj} is the time interval of fourth mode that are shown in Fig. 2.

2.1.5. Fifth Operating Mode ($t_3 \le t < t_4$):

The equivalent circuit of fifth mode for one stage is shown in Fig. 3(e). The capacitor C_{1j} is charged and the capacitor C_{2j} is discharged. Similar to first mode, the currents i_{Lm}, i_{Lk} and i_{L2} are considered equal to their initial values of I_{s1}, I_{m1} and I_{k1}, respectively. As a result, the time interval of the fifth mode (T_{5j}) is calculated as follows:

$$T_{5j} = \frac{n_j (C_{1j} + C_{2j}) V_H}{n_j I_{s1j} + I_{m1j} + (n_j - 1) I_{k1j}} \tag{9}$$

2.1.6. Sixth Operating Mode ($t_5 \le t < t_6$):

The equivalent circuit of this mode is shown in Fig. 3(f). This mode starts with ZVS turning on of the switch S_{2j}. The voltages across the inductors L_{mj}, L_{kj} and L_{sj} are equal to $(V_{\ell j} - V_H)/n_j$, $(n_j - 1)(V_{\ell j} - V_H)/n_j$ and $V_{C4} - V_H$, respectively. As a result, the inductors' currents are written as following equations:

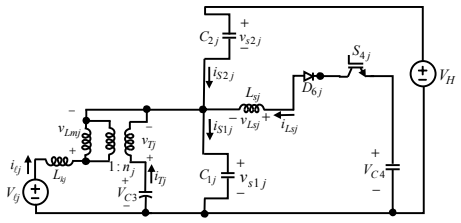
$$i_{Lmj} = \frac{(V_{\ell j} - V_H)}{n_j L_{mj}} (t - t_5) + I_{m1j} \tag{10}$$

$$i_{Lkj} = \frac{(n_j - 1)(V_{\ell j} - V_H)}{n_j L_{kj}} (t - t_5) + I_{k1j} \tag{11}$$

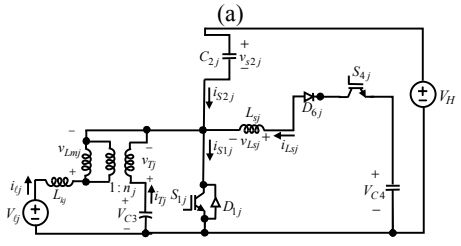
$$i_{Lsj} = I_{s1j} + \frac{(V_{C4} - V_H)}{L_{sj}} (t - t_5) \tag{12}$$

Considering (10)-(12) the current i_{S2j} is obtained as follows:

$$i_{S2j} = -\left(\frac{n-1}{n}\right) I_{k1} - \frac{I_{m1}}{n} - I_{s1} - \left[\left(\frac{n_j - 1}{n_j}\right)^2 \frac{(V_{\ell j} - V_H)}{L_{kj}} + \frac{(V_{\ell j} - V_H)}{n_j{}^2 L_m} + \frac{(V_{C4} - V_H)}{L_{sj}}\right](t - t_5) \tag{13}$$



(a)



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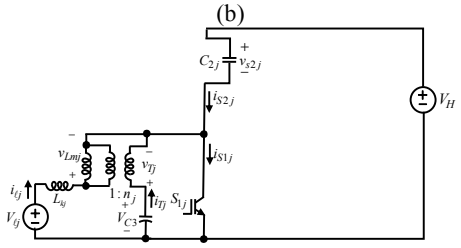

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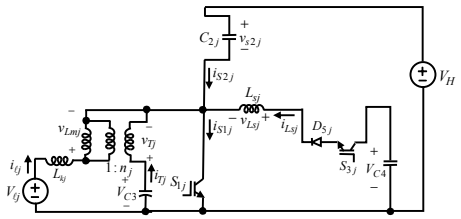

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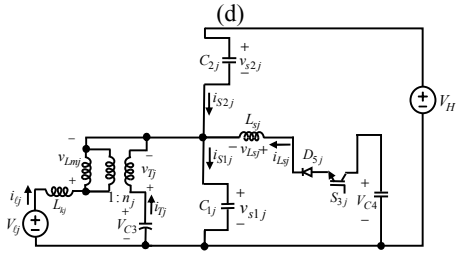

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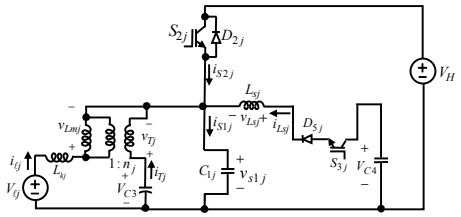
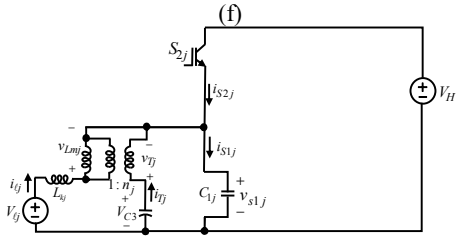
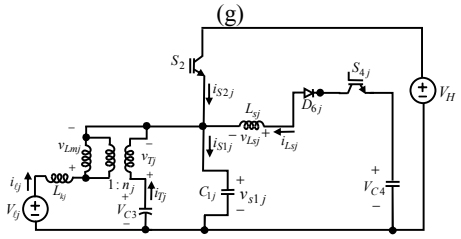


(f)



(g)



(h)

Fig. 3. The equivalent circuits of the proposed converter for one stage in boost operation.

2.1.7. Seventh Operating Mode ($t_6 \le t < t_7$):

The equivalent circuit of seventh mode for one stage is shown in Fig. 3(g). Similar to third mode, the current i_{Lsj} and voltage v_{Lsj} reach to zero. As a result, the switch S_3 is turned off at ZCS state.

2.1.8. Eighth Operating Mode ($t_7 \le t < t_8$):

The equivalent circuit of eighth mode for one stage is shown in Fig. 3(h). The voltage across the inductor L_{sj} is equal to $V_{C4} - V_H$. As a result, it can be written that:

$$i_{Lsj} = \frac{V_{C4} - V_H}{L_{sj}} (t - t_7) \tag{14}$$

2.2. Buck Operating Mode

In the buck mode, all of the voltages have the waveforms are the same as boost operation. The current waveforms of the proposed converter in buck mode for $n_j = 1$ (required condition for achieving free ripple input currents) are shown in Fig. 4. By comparing Fig. 2 and Fig. 4, it is resulted that the currents waveforms are similar to the boost operation and only the direction of currents L_m, L_k, S_1 and S_2 are changed. The equivalent circuits of the converter in buck operation are the

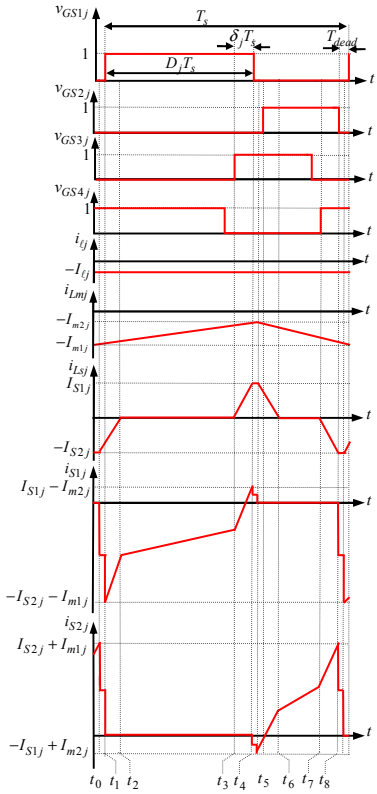


Fig. 4. Waveforms for buck operation.

same as the boost operation as shown in Fig. 3. The obtained results for buck operation are summarized in Table 1.

2.3. Auxiliary Capacitor Voltage Calculation

Based on the waveform of v_{Lsj} from Fig. 2 and by applying the voltage balance law for inductance L_{sj}, it can be written that :

$$(\delta T_s + \delta_{12} T_s) V_{C4} = (\delta T_s + \delta_{56} T_s)(V_H - V_{C4}) \quad (15)$$

Where, based on Fig. 2 $\delta_{12} T_s$ and $\delta_{56} T_s$ are the time intervals between t_1 to t_2 and t_5 to t_6, respectively. By considering the current balance law for C_4, it can be written that:

$$\frac{1}{2}(\delta T_s + \delta_{12} T_s) I_{s2j} = \frac{1}{2}(\delta T_s + \delta_{56} T_s) I_{s1j} \quad (16)$$

Considering (15)-(16) the voltage across the capacitor C_4 is calculated as follows:

$$V_{C4} = \frac{V_H}{2} \quad (17)$$

By replacing (17) into (8) the maximum and minimum currents values of I_{s1j} and I_{s2j} can be calculated as follows:

$$I_{s1j} = I_{s2j} = \frac{V_H}{2L_{sj}} \delta T_s \quad (18)$$

2.4. Main Inductors' Currents Calculation

Considering (3) and (11) the required condition for achieving zero input currents ripple is obtained as follows:

$$n_j = 1 \quad and \quad L_{kj} \neq 0 \quad (19)$$

By applying KCL at input bridge in Fig. 2, it is resulted that $i_{Lkj} - i_{Lmj} = -n_j i_{Lsj}$. Since the average value of current i_{Lsj} $(i_{C3j} = i_{Lsj})$ is equal to zero, the average value of input current $i_{\ell j}$ $(i_{Lkj} = i_{\ell j})$ is equal to average value of current i_{Lmj}. As a result, considering Fig. 2, it is obtained that $I_{\ell j} = (I_{m1j} + I_{m2j})/2$. Where, $I_{\ell j}$ is average value of input current $i_{\ell j}$. Considering Fig. 2, I_{m1j} and I_{m2j} are the maximum and minimum currents values of i_{Lmj}. Considering (7) and $n_j = 1$ it can be written that:

$$I_{m1j} = I_{\ell j} + \frac{V_{\ell j}}{2L_{mj}} D_j T_s \quad (20)$$

$$I_{m2j} = I_{\ell j} - \frac{V_{\ell j}}{2L_{mj}} D_j T_s \quad (21)$$

2.5. Voltage Gain Calculation

Based on voltage balance law of the inductor L_{mj} the average value of the voltage v_{Lmj} is equal to zero during a switching period. As a result, based on the waveform of v_{Lmj} from Fig. 2 and considering $n_j = 1$, it can be written that:

$$\frac{V_H}{V_{\ell j}} = \frac{1}{1 - D_j} \quad (22)$$

Where, $V_{\ell j}$ is the voltage source at low voltage side for each stages. D_j is the duty cycle of the main switch S_{1j} in each stages.

2.6. ZVS Condition for Main Switches

For achieving the zero voltage turning on of the switch S_{1j} at the beginning moment of second mode, at first the internal diode of this switch (D_{1j}) should be turned on. In another words, the current through this internal diode at the beginning of second mode should has a positive value. Therefore, the required conditions for ZVS operation of switch S_{1j} for boost operation can be written as follows:

$$i_{S1j}\big|_{t=t_1} < 0 \quad (23)$$

$$T_{dead} < T_{DS1j} \quad (24)$$

Where, T_{dead} is the dead time for the switches S_{1j} and S_{2j}. T_{Ds1j} is the interval time of conducting the diode D_{1j} at second mode. After this time the switch S_{1j} can be turned on at ZVS state. As a result, considering (5) and (19) it can be written that:

$$\left(\frac{V_{\ell j}}{L_{mj}} + \frac{V_{C4}}{L_{sj}}\right) T_{Ds1j} + I_{m2j} - I_{s2j} = 0 \quad (25)$$

By considering $T_{dead} = T_s/100$ and by replacing the values of I_{s2j} and I_{m2j} from (18) and (21) into (25) the required condition for ZVS operation of switch S_{1j} in boost mode is obtained as follows:

$$\delta T_{sj} > \frac{2L_{sj}(1-D_j)P_{\ell j}}{V_{\ell j}^{\,2}} - \frac{L_{sj}}{L_m}(1-D_j)\left(D_j - \frac{1}{50}\right)T_s + \frac{T_s}{100} \quad (26)$$

In boost operation, as shown in Fig. 2 the ZVS mode of switch S_{2j} is always existed. In the same way, the ZVS operation of switch S_{2j} in buck mode is obtained as follows:

$$\delta T_{sj} > \frac{2L_{sj}(1-D_j)P_{\ell j}}{V_{\ell j}^{\ 2}} - D_j\left(1-D_j-\frac{1}{50}\right)\frac{L_{sj}}{L_{mj}}T_s + \frac{T_s}{100} \qquad (27)$$

In buck mode, as shown in Fig. 4 the ZVS operation of switch S_{1j} is always existed.

Table 1. Summarized results for buck operation.

Operating Modes	Equations
1th Mode $(t_0 \le t < t_1)$	$T_{1j} = \dfrac{n_j(C_{1j}+C_{2j})V_H}{I_{m1j}+n_jI_{s2j}+(n_j-1)I_{k1j}}$
2th Mode $(t_1 \le t < t_2)$	$i_{S1j} = \left[\dfrac{(n_j-1)^2}{n_j^{\ 2}}\cdot\dfrac{V_{\ell j}}{n_jL_{kj}} + \dfrac{V_{\ell j}}{n_j^{\ 2}L_{mj}} + \dfrac{V_{C4}}{L_{sj}}\right](t-t_1) + \dfrac{(n_j-1)}{n_j}I_{k2j} - I_{s2j} - \dfrac{I_{m1j}}{n_j}$
3th Mode $(t_2 \le t < t_3)$	$i_{S1j} = \left[\left(\dfrac{n_j-1}{n_j}\right)^2\dfrac{V_{\ell j}}{L_{kj}} + \dfrac{V_\ell}{n_j^{\ 2}L_m}\right](t-t_5) + \left(\dfrac{n_j-1}{n_j}\right)I_{k2} - \dfrac{I_{m1j}}{n_j}$
4th Mode $(t_3 \le t < t_4)$	$-I_{m2j} = -I_{m1j} + \dfrac{V_{\ell j}}{n_jL_{mj}}D_jT_s$
5th Mode $(t_4 \le t < t_5)$	$T_{5j} = \dfrac{n_j(C_{1j}+C_{2j})V_H}{n_jI_{s1j}+I_{m1j}-(n_j-1)I_{k2j}}$
6th Mode $(t_5 \le t < t_6)$	$i_{S2j} = -\left(\dfrac{n_j-1}{n_j}\right)I_{k2j} - \dfrac{I_{m2j}}{n_j} - I_{s1j} - \left[\left(\dfrac{n_j-1}{n_j}\right)^2\dfrac{(V_{\ell j}-V_H)}{L_{kj}} + \dfrac{(V_{\ell j}-V_H)}{n_j^{\ 2}L_m} + \dfrac{(V_{C4}-V_H)}{L_{sj}}\right](t-t_5)$
7th Mode $(t_6 \le t < t_7)$	$i_{S2} = -\left(\dfrac{n_j-1}{n_j}\right)I_{k2j} - \dfrac{I_{m2j}}{n_j} - \left[\left(\dfrac{n_j-1}{n_j}\right)^2\dfrac{(V_{\ell j}-V_H)}{L_{kj}} + \dfrac{V_{\ell j}-V_H}{n_j^{\ 2}L_{mj}}\right](t-t_5)$
8th Mode $(t_7 \le t < t_8)$	$i_{Lsj} = \dfrac{V_{C4}-V_H}{L_{sj}}(t-t_7)$

3. Simulation Results

In order to reconfirm the validity of theoretical results, PSCAD/EMTDC simulation results are extracted. The used parameters in simulation are shown in Table 2. In the boost mode two stages have boost performance. Figs. 5(a) and 5(b) show the capability of ZVS for switches S_{11} and S_{12}, respectively. As shown in this figures, by turning on the auxiliary diodes of switches (D_{11} and D_{12}) their voltages (v_{s11} and v_{s12}) are equal to zero. In this condition, the trigger pulses of switches S_{11} and S_{12} are applied before the direction of currents i_{s11} and i_{s12} are changed. As a result, the switches can achieve zero voltage switching at their turning on moment. As mentioned before, considering Fig. 2 the ZVS performance of switches S_{21} and S_{22} are always existed for boost operation. Considering Figs. 5(a)-5(b) the voltage stresses on switches S_{11} and S_{12} are equal to $V_H = 80V$. Fig. 6(a) and 6(b) show the capability of ZCS turning off of the auxiliary switches S_{41} and S_{42}. In the same way, ZCS turning off of the auxiliary switches S_{31} and S_{32} can be shown. Considering Fig. 6, before the trigger pulses of the auxiliary switches are finished, the currents of these switches are reached to zero and ZCS turning off of the auxiliary switches are achieved. The voltage stresses on the auxiliary switches are lower than the output voltage V_H. Fig. 7(a) and 7(b) show the free ripple input currents at low voltage side for both stages. Fig. 8(a) and 8(b) show the output voltage V_H and voltage across the capacitor C_4, respectively.

Table 2. Used parameters for simulation.

$D = 0.6 and 0.7$	$C_{31} = C_{32} = 100\mu F$
$f_s = 50kHz$	$C_4 = 20\mu F$
$n_1 = n_2 = 1$	$L_{m1} = L_{m2} = L_m = 80\mu H$
$L_{s1} = L_{s2} = 90\mu H$	$L_k = 45\mu H$
$V_{\ell 1} = 24V$	$C_1 = C_2 = C_3 = C_4 = 0.00005\mu F$
$V_{\ell 2} = 32V$	$C_H = 100\mu F$
$R_H = 64\Omega$	

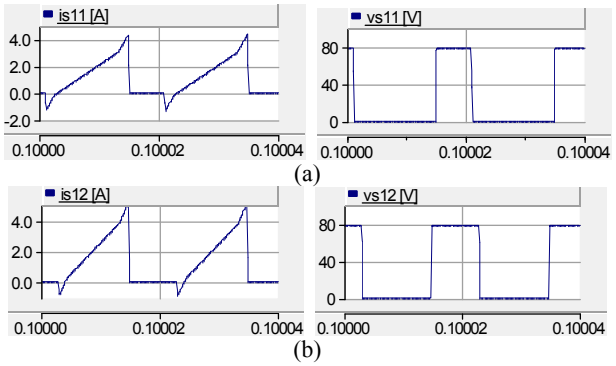


Fig. 5. ZVS operation of main switches for boost operation; (a) Voltage and current of the switch S_{11}; (b) Voltage and current of the switch S_{12}.

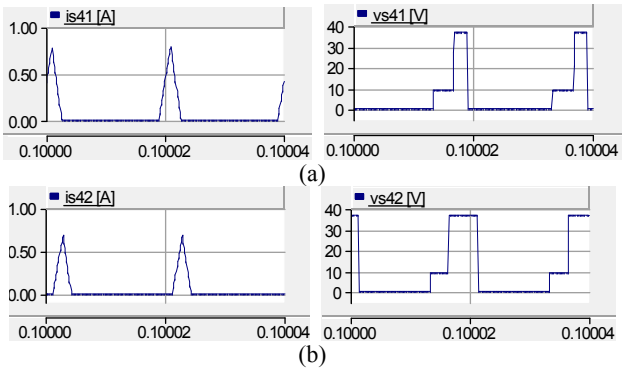


Fig. 6. ZCS operation of auxiliary switches for boost operation; (a) voltage and current of the switch S_{41}; (b) voltage and current of the switch S_{42}.

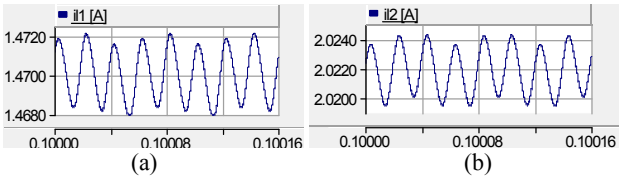
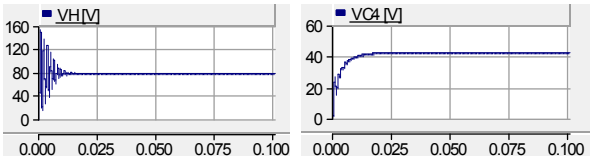


Fig. 7. Input currents; (a) Input current $i_{\ell 1}$; (b) Input current $i_{\ell 2}$.



(a) (b)

Fig. 8. (a) Output voltage V_H ; (b) Voltage V_{C5} .

4. Conclusion

In this paper, a new multiport non-isolated bidirectional dc-dc converter with capability of ZVS operation of main switches, ZCS operation of auxiliary switches and cancelling input currents ripple at low voltage side was proposed. By adjusting the value of auxiliary inductors of L_{s1} and L_{s2} and interval time of δT_{s1} and δT_{s2} the ZVS operation of main switches are achieved for different values of input powers of $P_{\ell 1}$ and $P_{\ell 2}$ in each stages. In this paper, the maximum and minimum currents through the switches, voltage stresses on switches, voltage gain, required condition for achieving ZVS operation of switches and required condition for cancelling input currents ripple at low voltage side has been calculated for both boost and buck operations. Finally, the analytical results were reconfirmed through the PSCAD/EMTDC simulation results.

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