Fully Integrated 98mV Start Up DC-DC Converter for Energy Harvesting in Batteryless IoT/Wearable Devices

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Abstract

Energy harvesting is an important pillar for large scale exploitation of IoT smart nodes and wearable devices. To this end, DC-DC converters with ultra-low start-up voltage, full integration and high efficiency in a wide input voltage range are required. In this paper a novel one-input, two-output DC-DC converter circuit is introduced. Low-power output provides 0.8-3.5 V with maximum load current of 3.5 µA starting up from 98 mV input. High-power output is turned on by an ultra-low-power voltage detector when input voltage reaches 150 mV, to provide 0.8-2.4 V with maximum load current of 200 µA. The circuit has been implemented in UMC 180-nm CMOS technology. Maximum simulated system efficiency is 34% at 0.2 V input. Low-power output meets the real time power demand of sensing, data processing and data storage blocks of IoT/Wearable devices, while high-power output provides sufficient power for data transmission, enabling batteryless operation.

1. Introduction

IoT smart nodes and wearable healthcare devices have recently been in the center of attraction for their fundamental role in future's smart world and healthcare systems. Large scale implementation however can only be feasible if their energy demand is met by means of tiny energy harvesters such as Thermoelectric Generators (TEG) and Photovoltaic Cells (PVC). Due to size and power restrictions imposed by the application, fully integrated DC-DC converters which can step up ultra-low voltage of harvesters, as low as 100 mV, to the levels that can empower target circuits, typically >700mV, with high power conversion efficiency (PCE) are of interest. Furthermore, eliminating any energy storage elements, such as battery or supercapacitor has been a desirable design objective offering prolonged maintenance-free life span [1]. Conventional inductive boost topology offers high efficiency and power, however required inductor size is in the range of µH which is not practical for on-chip realization. Ring oscillator with charge pump topology is a widely used alternative which offers an integrated solution, but has low start up and power efficiency for voltages <300mV due to MOSFET threshold voltage. An LC-Tank oscillator provides an effective solution for cold start-up. In [2], ring oscillator is replaced by an LC voltage-controlled oscillator (VCO) composed of four inductors and a capacitor, resulting in a converter with 140 mV start up voltage. However, it suffers from low efficiency of 20% because of lack of an optimization method. In [3], an enhanced swing inductive ring oscillator (ESIRO) is utilized with optimized size for minimum start up. The solution yields minimum start up voltage of 73 mV, but has 1% efficiency due to the use of power-hungry zero-threshold MOSFETs. In [4], two on-chip transformers are used to boost up the voltage swing of an LC VCO that feeds a 5 stage latched charge pump to achieve 0.4 V from 85 mV input. Due to the large transformer structures, calculated efficiency of this work is less than 1%. In [5], LC-tank is optimized, and charge pump from [7] is used with superior efficiency compared to the classical Dickson Charge pump, resulting in 22% efficiency with startup voltage of 0.2 V. [8] reports a model based optimization method for the charge pump and LC-tank structure that was introduced in [6]. Utilizing planar inductor instead of center tap structure decreases output impedance of the LC-Tank oscillator, resulting in higher current delivery to the charge pump circuit. 35% efficiency is achieved for 45 kΩ load in this design. 1.65 V output from 200 mV input voltage with startup as low as 150 mV is also achieved using the optimization method. LC-tank structure in all of the aforementioned papers is composed of four inductors, which increases layout area, and adversely affects efficiency. [9] reports use of an LC-tank oscillator with only two inductors which is a well know oscillator architecture introduced and analyzed in [10] as inductive load ring oscillator (ILRO). Based on the lumped half circuit model and proposed optimization method, the efficiency of 46% is achieved, for 0.2 V input and 6 kΩ load. Even though start up voltage is 100 mV for LC-tank in this paper, the large charge pump loading effect prevents oscillation for V_{in} < 150mV. In [11], a fully integrated converter that uses an LC-tank oscillator for start-up and a ring oscillator for normal mode is introduced. The converter starts up at 100 mV input, and boosts up to 760 mV with efficiency of 33.3%. However, this solution provides maximum 6.6µW output power in a very narrow input voltage band of 100 mV which is not sufficient for a batteryless application.

Power demand of a typical IoT node or a wearable device comes from 1) processing unit, 2) temporary data storage elements, 3) sensing nodes and 4) wireless data transmission unit. Wireless data transmission is the most power hungry part of the circuit. In this paper, a single input dual output DC-DC converter, based on ILRO, composed of two separate charge pumps with start-up voltage of 98 mV, and maximum design efficiency of 34% is presented. Start-up charge pump (SCP) supplies output voltage > 0.8 V to a 1 MΩ load starting from V_{DD}=98 mV. Output power of SCP is sufficient to activate sensing, computation and temporary storage circuits of a recent technology IoT node or

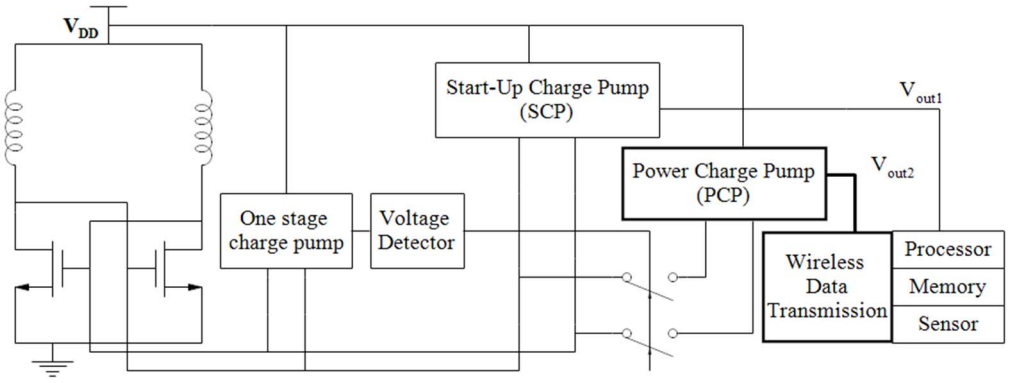


Fig. 1. The proposed DC-DC converter overall system topology

wearable device. Utilizing an ultra-low-power voltage detector, the power charge pump (PCP) autonomously starts power conversion when the input voltage reaches 150 mV. The generated power from PCP can meet real time power demand of recent technology transmission circuits [13]. This novel power supply paradigm would be of interest for real applications, where target circuits can use low power output to enable sensors, processing unit and data storage memory. Collected and processed data can be transmitted as soon as high power necessary for wireless transmission is supplied.

The rest of this paper is organized as follows: In section 2 the overall converter topology is discussed. Detailed charge pump optimization method for minimum startup and maximum voltage conversion ratio is covered in section 3. Section 4 discuses voltage detector circuit design. Section 5 covers simulation results and discussion. Finally, paper ends with concluding remarks in section 6.

2. Overall system topology

Ultra-low input voltage range of 98-300 mV is a typical generated output range of small thermoelectric generators or tiny solar PV cells when exposed to 2 K to 4 K temperature gradient or indoor light respectively. To harness this input voltage range, the circuit topology depicted in Fig. 1 is proposed. The novelty of this design is the optimization of two charge pumps with different MOSFET sizes that share a single LC-tank oscillator to provide both low-power and high-power output depending on input voltage level. The design enables batteryless operation, where data transmission is only started when sufficient input voltage (and power) is available.

The SCP boosts the input voltage range of 98-150 mV up to 0.8-1.6 V respectively, which directly meets the power demand of target sensing and processing circuits if not transmitting data. Once the input voltage reaches 150 mV, the voltage detection circuitry connects the PCP to LC-tank to supply the circuit with hundreds of microwatts of power with maximum efficiency of 34% to satisfy the high power demand of wireless data transmission circuits. For V_{DD} > 150mV, two charge pumps simultaneously convert voltage, sharing the same LC-tank oscillator. Voltage detector circuit, which is described in section 4, triggers high output voltage when its input voltage reaches a specific threshold (trigger). The voltage detector circuit is composed of two P-type MOSFETs operating in subthreshold region with power consumption of a few nWs. To boost up input voltage to a detectable level by this circuit, a single stage charge pump is implemented that upconverts 150 mV input to 360 mV.

3. Start-up charge pump design

Design goals for the DC-DC converter optimization could be either 1) minimum start up voltage, 2) maximum output voltage, 3) maximum efficiency, or a combination of all three. Ambient energy harvesters typically produce varying voltages. Therefore, energy harvesting interfaces should be operable within a wide input voltage range to provide a reliable power source for target circuits. This is more critical when the application requires use of hybrid sources with different voltage ranges. Achieving all the aforementioned goals with a single charge pump is hardly feasible. Minimum start up voltage and maximum output voltage constraints are considered in the SCP design, while maximum efficiency is delivered with the PCP design. LC-tank and PCP sizes are preserved the same as proposed previously by our group in [8], which are optimal values for maximum efficiency. Therefore, only NMOS and PMOS sizes of SCP need to be determined as design parameters. Fig. 2 shows the LC-tank small signal model with charge pump modeled as the load. Calculating the transfer function using this model results in equation for minimum start up condition. Transfer function is given in (1).

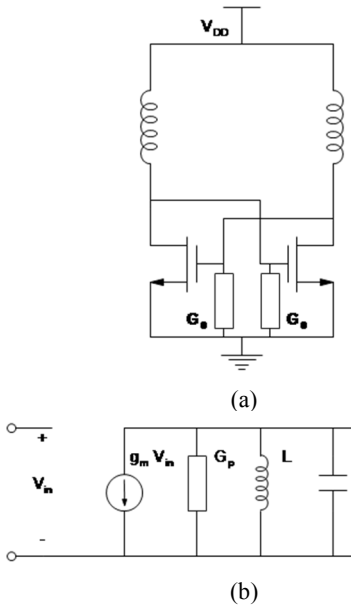


Fig. 2. (a) LC-tank with charge pump modeled as the load, (b) small signal model of the circuit shown in (a)

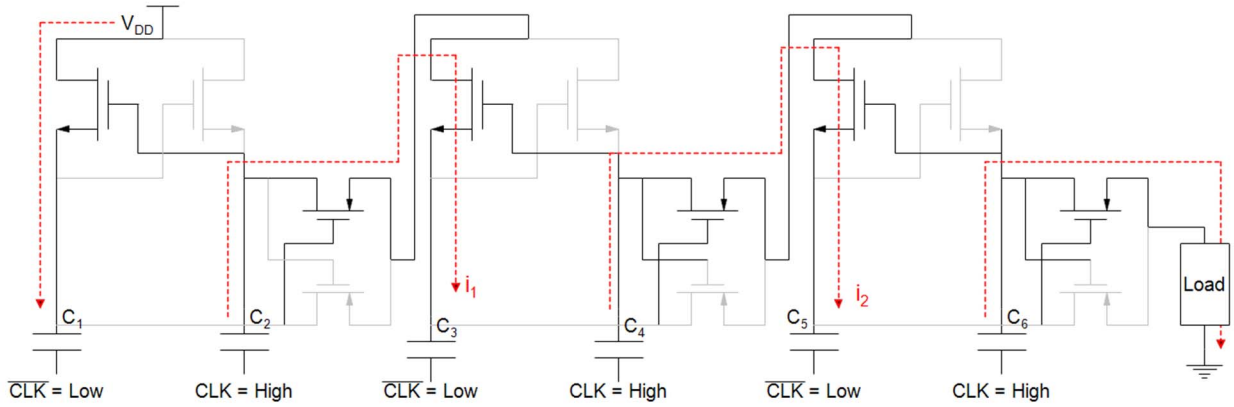


Fig. 4. ON and OFF elements in a 3 stage charge pump at the time CLK=High

$$\frac{V_{out}}{V_{in}} = -g_m\left(\frac{G_p+G_0}{(G_p+G_0)^2+\left(\frac{1}{L\omega}-C\omega\right)^2}+\frac{\frac{1}{L\omega}-C\omega}{(G_p+G_0)^2+\left(\frac{1}{L\omega}-C\omega\right)^2}j\right) \quad (1)$$

where g_m represents MOSFET transconductance, G_p is the inductor conductance, modeling the non-ideal inductor, G_0 models the charge pump load. L, C and ω are the inductance, capacitance and oscillation frequency. C represents NMOS gate-drain and drain-source capacitances. The phase shift $\emptyset$ between V_{out} and V_{in} is derived from (1) as

$$\emptyset = \pi - tan^{-1}\left(\frac{\frac{1}{L\omega}-C\omega}{G_p+G_0}\right) \quad (2)$$

Oscillation condition requires that $\emptyset = \pi$ [9]. Therefore, oscillation frequency calculated from (2) is

$$\omega = \frac{1}{\sqrt{LC}} \quad (3)$$

In addition, start up condition requires greater-than-unity gain [9], which results in the minimum oscillation start-up condition,

$$g_m > G_p + G_0 \quad (4)$$

Fig. 3 shows the lumped circuit model for LC-tank and n-stage charge pump introduced in [8].

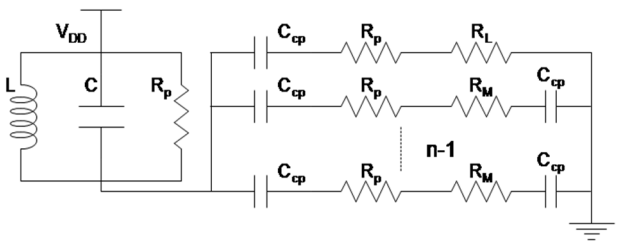


Fig. 3. Lumped circuit model for LC-tank and n stage charge pump circuit proposed in [8]

G_0, admittance of the charge pump, can be calculated from this model as:

$$G_0 = \frac{1}{Z_{cp}} = \frac{R_L+R_p}{(R_L+R_p)^2+\left(\frac{1}{C_{cp}\omega}\right)^2}+(n-1)\frac{(R_M+R_p)}{(R_M+R_p)^2+\left(\frac{2}{C_{cp}\omega}\right)^2} \quad (5)$$

$$+j(C_{cp}\omega)\left(\frac{1}{1+(C_{cp}\omega)^2(R_L+R_p)^2}+\frac{2\,(n-1)}{4+(C_{cp}\omega)^2(R_M+R_p)^2}\right)$$

where R_P, R_M are charge pump PMOS and NMOS average switching resistance respectively, n is the number of stages and R_L is the charge pump load. It is worth emphasizing that g_m and G_0 values depend on V_{DD}, but G_p, modeling L non-ideality, is almost constant. G_p can be calculated knowing the quality factor of the inductor, G_0 comes from (5). Fig. 5 shows simulated g_m values for the oscillator cross coupled NMOS pair for different input voltage values.

To better understand output voltage equation of the DC-DC converter with n number of stages, ON and OFF paths in a 3 stage charge pump for $CLK = high$ is illustrated in Fig. 4.
C_1 charges to $V_{DD} - V_{ND}$, where V_{ND} represents voltage drop across NMOS. C_3 charges to $V_{OSC} + V_{C_2} - V_{ND} - V_{PD}$, where V_{PD} represents voltage drop across PMOS. From the schematic, $V_{C_{2n-1}} = V_{C_{2n}}$, where n is the number of stages and V_C represents the maximum voltage across the capacitor. The circuit has 2 time constants, $R_M C$ and $\frac{1}{2}(R_M + R_P)C$. The dominant time constant determines the upper bound of the oscillation frequency in LC-tank design. Voltage, to which C_{2n} will be charged, can be calculated by solving (6).

$$V_{C_{2n}} = (n-1)V_{osc} + V_{DD} - n\,V_{ND} - (n-1)V_{PD} - \frac{Ti_n}{2C} \quad (6)$$

Where i_n is the output current of stage n. V_{osc} is the maximum LC-tank oscillation voltage. Output voltage can be calculated from (6) as:

$$V_{out} = (V_{osc} + V_{C_{2n}})\,e^{-\frac{T}{4(R_L+R_P)C}} \times \frac{R_L}{R_L+R_P} \quad (7)$$

Minimum start-up for the oscillator proposed in [8] is 98 mV. G_0 of the SCP must satisfy the minimum start up condition given by (4). To this end, (5) requires that R_M and R_P have higher values,

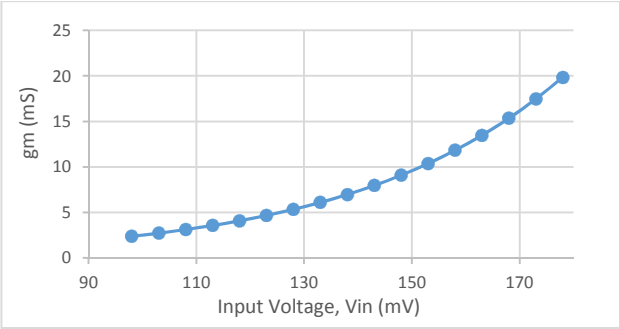


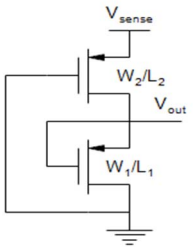
Fig. 5. Oscillator cross coupled NMOS pair transconductance simulation results for different input values

which results in smaller MOSFET size. Considering R_M and R_P proposed in [8], g_m and G_p values, NMOS and PMOS widths can be calculated. In addition, decrease in G_0 results in higher oscillation amplitude due to higher gain according to (1). Decreasing MOSFET size further, increases V_{ND} and V_{PD} that reduces output voltage and efficiency.

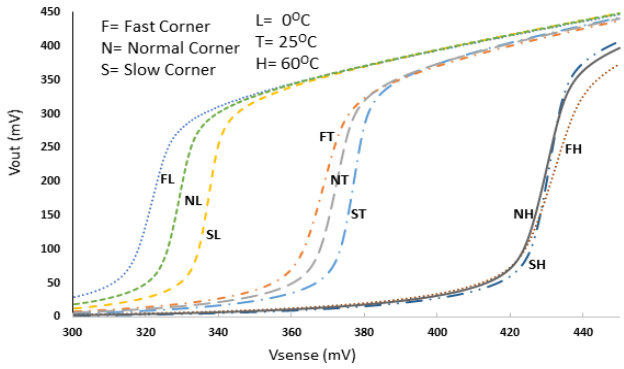
4. Ultra-low power voltage detector design

In order to detect input voltage value and autonomously connect PCP, ultra-low power voltage detector circuit proposed in [12] is utilized. Trigger voltage for the circuit, depicted in Fig. 6 (a), can be calculated using (8).

$$V_{Trigger} = \frac{mkT}{q} ln\left(\frac{W_1}{W_2} \times \frac{L_2}{L_1}\right) \quad (8)$$



(a)



(b)

Fig. 6. (a) Ultra-low power voltage detector circuit, (b) V_{out} vs V_{sense} curve with respect to temperature and process variations for the circuit shown in (a).

Conventionally, voltage reference circuits with comparators are used for voltage level detection. Comparators are active elements that need bias current, which increases their power dissipation from hundreds of nWs to some µWs. Instead, circuit shown in Fig. 6 (a) offers ultra-low power consumption due to operating in subthreshold region. The drawback of circuits operating in subthreshold region is sensitivity to temperature and process variations (PV). Fig. 6 (b) depicts simulation results, V_{out} vs V_{sense}, with respect to temperature and process variations for this circuit. Impact of PV is insignificant compared to temperature variation. Minimal design, using only two P-type MOSFETs, contributes to minimizing the impact of PV. Low temperature shifts trigger voltage left causing PCP to turn on for V_{DD} <150 mV while high temperature has the opposite effect. This trend complies with the application requirements. When the ambient temperatures deviates further from body temperature, higher temperature gradient available for TEG increases the input voltage and power. For high ambient temperature however due to adverse effect of temperature on MOSFET performance PCP turns on for higher input voltages which increases system reliability.

In order to make this circuit capable of sensing ultra-low voltage range, a one stage charge pump with minimum G_0 and power dissipation, is utilized that upconvertes input voltage to a detectable level. After the detector triggers, NMOS switches turn ON, connecting the PCP to LC-tank Oscillator.

5. Results and discussion

The circuit is simulated using UMC-180nm CMOS technology. Fig. 7 shows simulation results of SCP and PCP output voltage versus input voltage. Fig. 8 depicts efficiency of the PCP and the overall efficiency, which is the addition of PCP and SCP efficiencies. Load resistance for SCP and PCP is 1 MΩ and 12 kΩ respectively. Table 1 shows comparison of this work to the state of the art in the literature.

Output voltage of the SCP reaches 3.5 V when input is 300 mV while minimum boosted voltage is 0.8 V when input is 98 mV. PCP output also starts from 0.8 V when input voltage is 150 mV and reaches 2.4 V when input is 300 mV. As expected, SCP efficiency is very low compared to PCP efficiency, but it offers maximum voltage boost up gain and minimum start up volatge of 98 mV as was the design goal.

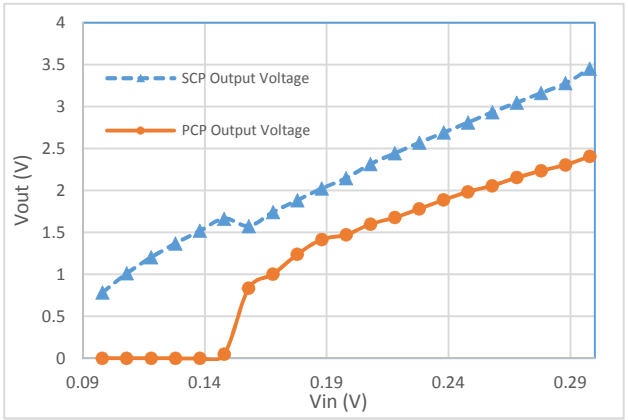


Fig. 7. Simulation results of SCP and PCP output voltage versus input voltage. SCP load is 1 MΩ and PCP load is 12 kΩ.

Table 1. Comparison of this work with state-of-the-art fully integrated DC-DC converters with LC-tank oscillator

	[1]	*[2]*	*[3]*	*[8]*	*[10]*	*This Work*
Process (nm)	180	130	65	180	65	180
Min Start-up Voltage (mV)	140	86	85	110 (no load), 150 (with load)	100	98
Min Output Voltage (V)	0.7	1	0.4	0.9	0.7	0.8
Maximum Output Current (µA)	15	1	2	283	8.6	200
Max Power Conversion Efficiency (%)	22	1	<1	46.5	33	34
LC-tank Type	4 inductors + 1 capacitor	4 inductors	2 transformers	2 inductors	2 inductors As start-up circuit only	2 inductors

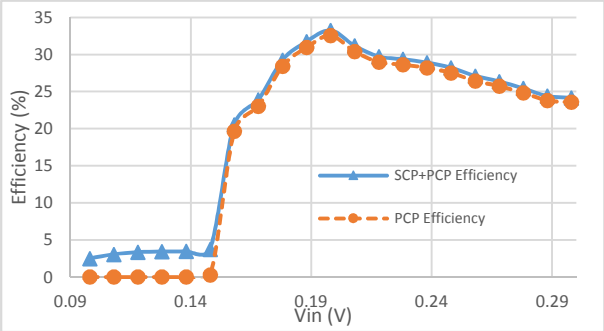


Fig. 8. Efficiency of the PCP and the overall efficiency which is the addition of PCP and SCP

6. Conclusions

A single input, dual output fully integrated DC-DC converter is proposed. Start-up voltage of 98 mV, high efficiency and wide input voltage range in addition to full integration makes this circuit suitable for energy harvesting with tiny thermoelectric generators, small indoor solar PV cells as well as hybrid energy harvesters in IoT and wearable devices. Matching the power levels from the two outputs of the proposed DC-DC converter with the power demand of processing and transmission modes of a typical IoT smart nodes and wearable devices facilitates the elimination of batteries or other bulky storage elements. The circuit delivers the best performance in literature in terms of lowest start-up voltage for the given (high) output power capacity.

7. References

[1] Muhtaroğlu. Ali, "Micro-scale Energy Harvesting for Batteryless Information Technologies", Energy Harvesting and Energy Efficiency, pp. 63-85. Springer International Publishing, 2017.

[2] Bassi, Giovanni, Luigi Colalongo, Anna Richelli, and Zsolt Miklós Kovacs-Vajna, "100 mV–1.2 V fully-integrated DC–DC converters for thermal energy harvesting", *IET Power Electronics,* vol. 6, no. 6, pp. 1151-1156, 2013.

[3] Machado, Marcio Bender, Marcio Cherem Schneider, Mohamad Sawan, and Carlos Galup-Montoro, "Fully-integrated 86 mV–1V step-up converter for energy harvesting applications", *New Circuits and Systems Conf. (NEWCAS)*, 2014, pp. 452-455.

[4] Fuketa, Hiroshi, Youichi Momiyama, Atsushi Okamoto, Tsuyoshi Sakata, Makoto Takamiya, and Takayasu Sakurai, "An 85-mV input, 50-µs startup fully integrated voltage multiplier with passive clock boost using on-chip transformers for energy harvesting", *European Solid State Circuits Conference (ESSCIRC)*, 2014 , pp. 263-266.

[5] Pathirana, W. P. M. R., H. M. P. C. Jayaweera, and Ali Muhtaroğlu, "Low input voltage and high step-up integrated regulator for thermoelectric energy harvesting", *Energy Aware Computing Systems & Applications (ICEAC)*, 2015 , pp. 1-4.

[6] Jayaweera, H. M. P. C., W. P. M. R. Pathirana, and Ali Muhtaroğlu, "Fully Integrated Ultra-Low Voltage Step-up Converter with Voltage Doubling LC-Tank for Energy Harvesting Applications", *Journal of Physics: Conference Series*, vol. 660, no. 1, p. 012017. IOP Publishing, 2015.

[7] Bhalerao, Shantanu A., Abhishek V. Chaudhary, and RajendraM. Patrikar, "A CMOS low voltage charge pump", *VLSI Design*, *Held jointly with 6th International Conference on Embedded Systems*, pp. 941-946, 2007.

[8] Jayaweera, H. M. P. C., W. P. M. R. Pathirana, and Ali Muhtaroğlu, "An on-die ultra-low voltage DC–DC step-up converter with voltage doubling LC-tank", *Journal of Micromechanics and Microengineering,* vol. 26, no. 12, p. 124010, 2016.

[9] Jayaweera, H. M. P. C., and Ali Muhtaroğlu, "Design optimization of a fully integrated charge-pump with LC tank oscillator for ultra-low voltage energy harvesting", *Microelectronics Journal, vol.* 59, pp .33-39, 2017.

[10] Machado, Marcio Bender, Marcio Cherem Schneider, and Carlos Galup-Montoro, "On the minimum supply voltage for MOSFET oscillators", *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 61, no. 2, pp. 347-357, 2014.

[11] Fuketa, Hiroshi, and Takashi Matsukawa, "Fully Integrated, 100-mV Minimum Input Voltage Converter With Gate-Boosted Charge Pump Kick-Started by LC Oscillator for Energy Harvesting", *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 4, pp. 392-396, 2017.

[12] Chen, Po-Hung, Koichi Ishida, Katsuyuki Ikeuchi, Xin Zhang, Kentaro Honda, Yasuyuki Okuma, Yoshikatsu Ryu, Makoto Takamiya, and Takayasu Sakurai, "Startup Techniques for 95 mV Step-Up Converter by Capacitor Pass-On Scheme and V_{TH}-Tuned Oscillator With Fixed Charge Programming", *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1252-1260, 2012.

[13] Intaschi, Luca, Paolo Bruschi, Giuseppe Iannaccone, and Francesco Dalena, "A 220-mV input, 8.6 step-up voltage conversion ratio, 10.45-µW output power, fully integrated switched-capacitor converter for energy harvesting", *Custom Integrated Circuits Conference (CICC)*, pp. 1-4, 2017.