Fully Integrated Ultra-Low Voltage DC-DC Converter with Voltage Quadrupling LC Tank Oscillator for Energy Harvesting Applications

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Abstract

This paper presents a novel fully integrated ultra-low voltage DC-DC converter and its multi-stage architecture. DC-DC converter frequency has been analytically derived using model analysis and validated in Cadence environment. The proposed voltage quadrupling LC tank oscillator eliminates the buffer circuits utilized in the traditional DC-DC converter, hence improves the performance metrics such as efficiency and output power capacity. The circuit was designed in 180nm standard CMOS process and was simulated to self-start and boost 70 mV to deliver 1.4 V to a 1 MΩ load. The minimum start-up voltage of the DC-DC converter is 60 mV. The optimized 2-stage DC-DC converter can yield 1.1 V output and 560 µW load power with 43% peak efficiency at 0.2 V input. The 3-stage and 4-stage can deliver 1524 µW and 1193 µW load power, 1.64 V and 2.18 V output voltage with 40% and 34% peak efficiency respectively at 0.2 V input.

1. Introduction

Smart low power low-cost devices are in trend for applications in Internet of Things (IoT) [1], wireless smart sensor networks, and implantable bio medical and health care devices [2]. A smart electronic device contains a power source, such as a button cell battery, which largely dominates the volume of the package [3]. Use of battery is impractical for some applications, such as implantable wireless body sensor network [4] and embedded smart sensors, where battery replacement is impossible or expensive. Therefore, battery is not a sustainable solution as the power supply for smart consumer electronic devices. In the recent decade, ambient thermoelectric or photovoltaic energy harvesting has become feasible as an alternative power source for low power microelectronic smart devices.

The generated voltage from a micro-scale ambient energy harvester is typically at the ultra-low range [5], [6] (≤ 200 mV), and is not sufficient to supply a standard load, even when there is sufficient power. An interface circuit is necessary to boost-up the harvester output before feeding into the load. A voltage step-up interface circuit for the fore mentioned DC sources is therefore needed. Existing ultra-low voltage on-chip DC-DC converters suffer from low efficiency, low voltage gain and output power capacity. Hence, there is significant research to enhance the performance of the ultra-low voltage integrated DC-DC converters, while down scaling the cold startup voltage.

2. Overview

Different DC-DC converter circuit topologies are available in the literature, including non-inductive and inductive circuits. Most early integrated DC-DC converters used non-inductive ring oscillators [7] to generate clock control to stimulate a charge pump. In addition to having a unity gain, the ring oscillator fails to operate at ultra-low voltage input (below the threshold voltage of the CMOS technology). The ring-type oscillators also require a large number of power-hungry buffer circuits to generate the necessary differential clock signals with sufficient drive to switch charge pump capacitors. Inductive converters with LC tank oscillators provide an attractive alternative for ultra-low voltage applications due to the high voltage gain, lack of buffer circuit, and enhanced cold start-up. There are a number of existing LC tank oscillator designs that can be used for DC-DC converter applications, including PMOS monolithic LC tank VCO [8], PMOS and NMOS cross-coupled LC tank VCO [9]. However, the PMOS cross-coupled structure suffers from low voltage gain (voltage gain ≤ 1) and fails to operate at ultra-low voltage due to the threshold voltage of the PMOS. The NMOS cross –coupled LC tank [10] overcomes the threshold voltage limitation and achieves a higher amplitude gain even at ultra-low input voltage range. However, the integrated LC tank oscillators suffer from low charge drivability, low oscillation purity, high impedance and limited amplitude gain (typical gain ≤ 2.5). As a result, a DC-DC converter with a conventional integrated LC tank oscillator achieves power efficiency ≤ 20% and load power ≤ 100 µW at ultra-low voltage operation for ≤ 10 kΩ load [11]. This paper proposes a novel LC tank design with superior cold startup performance, high oscillation purity, and high oscillation amplitude for DC-DC converter applications.

Different switched capacitor charge pump topologies are available in literature including CMOS implementation of the Dickson charge pump [12]. However, the Dickson topology is not feasible for the ultra-low voltage operation due to the reverse charge flow and threshold voltage limitation. A large number of MOSFETs available in a single stage of NCP topology[13] reduce the output voltage through body effect and leakage current, and hence not suitable for the ultra-low voltage operation. The NMOS cross-coupled and PMOS cross-coupled charge pump proposed by [14] provide a higher performance in ultra-low voltage operation due to the less number of MOSFETs in a single stage and maintains DC output during the entire clock period. Hence, it is the topology used in this work with suitable device parameters for low input voltage and high power performance.

The voltage quadrupling LC tank is a novel design for energy harvesting applications; hence an analytical model for this type of oscillator, or its interaction with the charge pump is lacking in the literature. The rest of the paper is organized as follows: Section 3 presents the DC-DC converter design and operation. The proposed multi-stage DC-DC converter is also presented in the same section. The model based circuit analysis is presented in section 4. The frequency response of the proposed DC-DC converter along with model validation and design characteristics curves are presented in section 5. Finally, section 6 discusses the conclusion of this work.

3. DC-DC converter design

Two identical and out-of-phase clock signals are necessary for the charge pump switch control. Low self-starting voltage, high gain and purity, low phase noise, and low internal impedance are desirable characteristics of the oscillator. The proposed voltage quadrupling LC tank oscillator has low internal impedance and most other characteristic necessary for ultra-low voltage DC-DC converter applications. The oscillator consists of four on-die inductors, two capacitors, and single cross-coupled NMOS pair. Each stage of the charge pump consists of NMOS cross-coupled pair and PMOS cross- coupled pair with two flying capacitors for charge storage and delivery to next stage according to the switching of the MOSFETs. The single stage DC-DC converter is composed of voltage quadrupling LC tank coupled with single stage charge pump as illustrated in Fig. 1. L_1 and C_{L1} form the primary LC tank along with the cross-coupled M_1 and M_2. The inductor stores energy in the form of magnetic flux, and capacitor stores energy as a charge. Fully charged capacitor tends to stop the current through the capacitor while generating a maximum voltage across it. However, the fully magnetized inductor allows maximum current while working as a short circuit path. The inductor resists the change of current through it. Once the capacitor is fully charged, the capacitor tends to stop the current through it. As a result, the fully charged inductor starts to produce a current through the capacitor in the same direction, and accumulate the charge on the capacitor while discharging the magnetic energy on L.

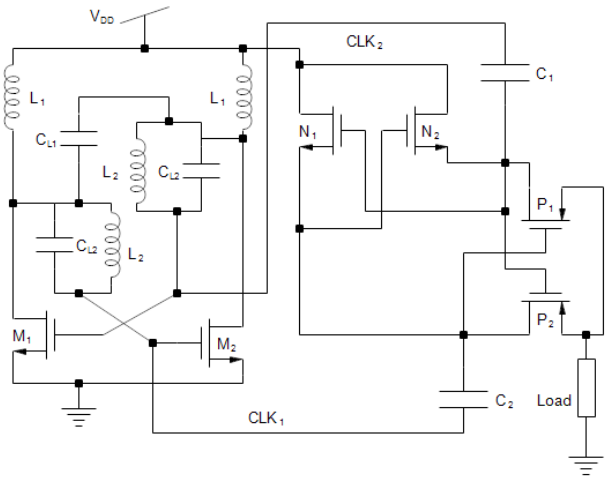

Fig. 1. Single-stage DC-DC converter with voltage quadrupling LC tank.

Finally, the primary capacitor will achieve > V_{DD} and < $2V_{DD}$ depending on the inductor energy loss. Since the external power source is in series with fully charged C_{L1}, the oscillator drain voltage will reach > 2 V_{DD} and < $3V_{DD}$. Hence, the voltage of the primary LC tank output oscillates between 0 V and $3V_{DD}$. The secondary LC tank consists of the L_2 inductor and C_2 capacitor along with the cross-coupled M_1 and M_2. Similar to primary LC tank, the C_2 capacitor will charge to $2V_{DD}$ with respect to the oscillator NMOS drain. M_1 and M_2 switching configuration allows charging C_2 to V_{DD} while the corresponding drain voltage is at $3V_{DD}$ peak voltage. As a result, the oscillator MOSFET gate will achieve $4V_{DD}$ peak amplitude and is the output of the oscillator. Once oscillator drain is at 0 V, the C_2 capacitor will achieve its negative peak voltage of $2V_{DD}$ and generate $-2V_{DD}$ at the output terminal. Therefore, the oscillator output oscillates between $-2V_{DD}$ and $4V_{DD}$, creating $6V_{DD}$ peak to peak amplitude.

CLK_1 and CLK_2 drive the charge pump MOSFETs to accumulate charge on the charge pump capacitors and transfer them to the next stage. Once CLK_1 is high, P_1 is off and N_2 is switched on, and allow accumulation of charge on C_1. Simultaneously, N_1 will be switched off while P_2 is on and will allow transfer of the accumulated charge through P_2. Since CLK_1 is at high stage ($4V_{DD}$) and in series with the fully charged C_2 (during the previous clock cycle C_2 will charge to V_{DD}) the output of the first stage will achieve $5V_{DD}$. During the next clock half cycle, the fully charged C_1 will be in series with the peak CLK_2 and will achieve $5V_{DD}$ at the output of the first stage. Hence, the output of the first stage will stay in a constant voltage during the entire clock cycle.

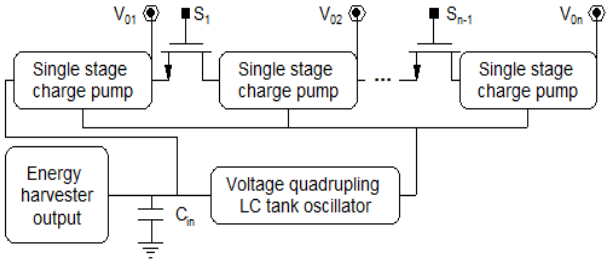

Fig. 2. Proposed multi-stage DC-DC converter for ultra-low voltage DC-DC converter applications.

Fig. 2 shows the block diagram of n-stage of multi-stage DC-DC converter for the ultra-low voltage applications. Each stage is connected through the switching NMOS and stage selection is controlled by this switches. For example, the S_2 switch ground allows disconnecting the higher stages and V_{02} will give the 2-stage output if S_1 is connected to V_{02}. Therefore, the system does not require any external voltage to select the required stage except the DC-DC converter input.

4. Modal based circuit analysis

The simplified small-signal half circuit model is shown in Fig. 3 for the frequency analysis. The primary LC tank model consists of the ideal components of C1 capacitor (C1 = C_{L1} + total parasitic capacitor at NMOS drain), L_1 inductor and R_{P1} equivalent parallel resistor of the L_1 series resistor. The L_2 is in series with the resistor, which is the self-resistance of L_2 and both parallel with C2 capacitor (C2 = C_{L2} + total parasitic capacitor across the L_2 inductor) to represent the secondary resonator. C_L represents the total capacitance at oscillator gate terminal (output of the oscillator) with respect to the AC ground including the

corresponding equivalent parallel capacitance of the charge pump. The oscillator frequency response with the load resistance is negligible. Charge pump total resistance is ignored for simplicity.

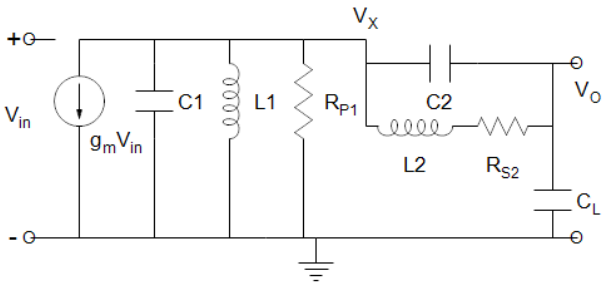

Fig. 3. Simplified small signal half circuit model of the DC-DC converter for frequency analysis.

The ratio of the output voltage (V_0) and the oscillator NMOS drain voltage (V_x) can be simply written as,

$$\frac{V_0}{V_x} = \frac{(1-\omega^2 L_2 C2)(1-\omega^2 L_2 C_0) + \omega^2 R_{s2}^2 C_0 C2}{(1-\omega^2 L_2 C_0)^2 + \omega^2 R_{s2}^2 C_0^2}, \quad (1)$$

where $C_0 = C2 + C_L$. Using the following assumptions,

$$(1-\omega^2 L_2 C_0)^2 \gg \omega^2 R_{s2}^2 C_0^2 , \quad (2)$$

$$(1-\omega^2 L_2 C2)(1-\omega^2 L_2 C_0) \gg \omega^2 R_{s2}^2 C_0 C2 , \quad (3)$$

equation (1) can simplify as,

$$\frac{V_0}{V_x} = \frac{1-\omega^2 L_2 C2}{1-\omega^2 L_2 C_0} . \quad (4)$$

The transfer function is,

$$\frac{V_0}{V_{in}} = \frac{-g_m}{\frac{(1-\omega^2 C_0 L_2)}{(1-\omega^2 L_2 C2) R_{p1}} + jA} , \quad (5)$$

$$A = \frac{(1-\omega^2 C_0 L_2)}{(1-\omega^2 L_2 C2)} \left(\omega C1 - \frac{1}{\omega L_1}\right) - \omega C_L \quad (6)$$

The phase shift between Vo and V_{in} should be π, Therefore, the frequency can be derived using the imaginary component of equation (5) as,

$$\omega^2 = \frac{b \pm \sqrt{b^2 - 4L_1 L_2 [C1C2 + C_L(C1+C2)]}}{2L_1 L_2 [C1C2 + C_L(C1+C2)]}, \quad (7)$$

$$b = L_1 C1 + L_2 C2 + C_L(L_1 + L_2) . \quad (8)$$

$$b^2 \geq 4L_1 L_2 [C1C2 + C_L(C1+C2)] . \quad (9)$$

Equation (7) yields two positive solutions for ω, but ω should satisfy the relation of

$$\omega^2 < \frac{1}{L_2(C2 + C_L)} , \quad (10)$$

for the oscillation voltage gain greater than unity in equation (4). Therefore,

$$\omega = \sqrt{\frac{b - \sqrt{b^2 - 4L_1 L_2 [C1C2 + C_L(C1+C2)]}}{2L_1 L_2 [C1C2 + C_L(C1+C2)]}} . \quad (11)$$

According to the equation (5), the minimum transconductance for the continuous oscillation is given by,

$$g_m = \frac{(1-\omega^2 L_2 C2 - \omega^2 C_L L_2)}{R_{P1}(1-\omega^2 L_2 C2)} . \quad (12)$$

5. Result and discussion

The peak amplitude of the voltage quadrupling LC tank oscillator has a proportional variation with a secondary LC tank capacitor, it is adverse relation to the primary LC tank capacitor as shown in Fig. 4. For the primary LC tank capacitance variation, C2 is 25 pF and for secondary LC tank capacitance variation C1 is 14 pF.

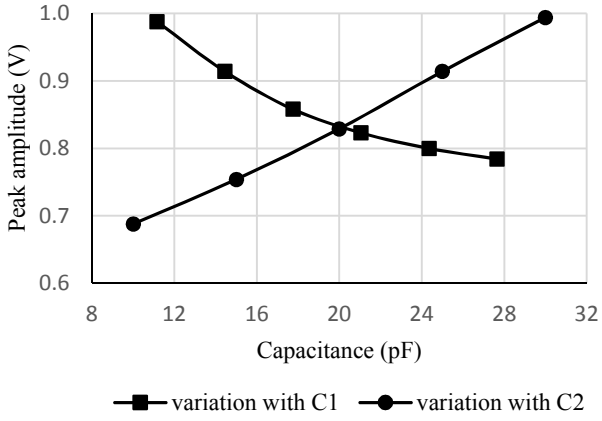

Fig. 4. The variation of voltage quadrupling LC tank peak amplitude with primary and secondary LC tank capacitors at 0.2 V input.

The variation of the oscillation frequency with the primary LC tank capacitor at C2 = 24 pF and secondary LC tank capacitor at C1= 11 pF is shown in Fig. 5 along with the model validation. Both primary and secondary capacitors decrease the DC-DC converter oscillation frequency while sustaining oscillations at < 300 MHz and > 150 MHz. Fig. 6 illustrated the DC-DC converter output voltage response with load resistance for different stages at 0.2 V input. The 4-stage DC-DC converter can achieve 2.2 V for 4 kΩ load resistance at 0.2 V input. The 4-stage DC-DC converter achieves the steady state operation for the load resistance ≥ 4 kΩ. However, the minimum load resistance for the steady state operation is increased with the DC-DC converter stages. Therefore, the 2-stage DC-DC converter can boost 0.2 V into 1.1 V for 1 kΩ load resistor. Despite the higher LC tank peak amplitude for larger secondary capacitor, the DC-DC converter output voltage is higher for the 10 pF secondary LC tank capacitor than the 25 pF secondary LC tank capacitor due to the partial charging and discharging of the flying capacitors.

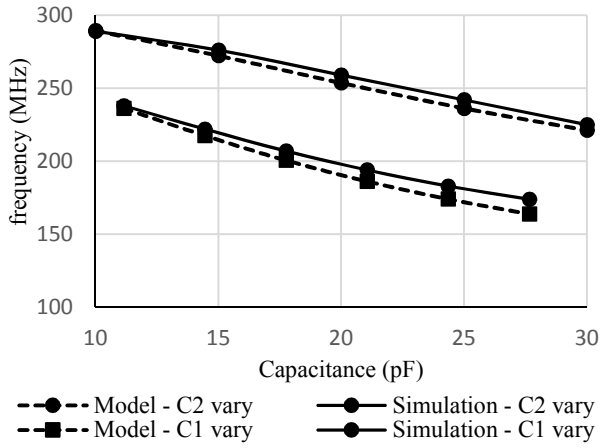

Fig. 5. The variation of DC-DC converter oscillation frequency with primary and secondary capacitance.

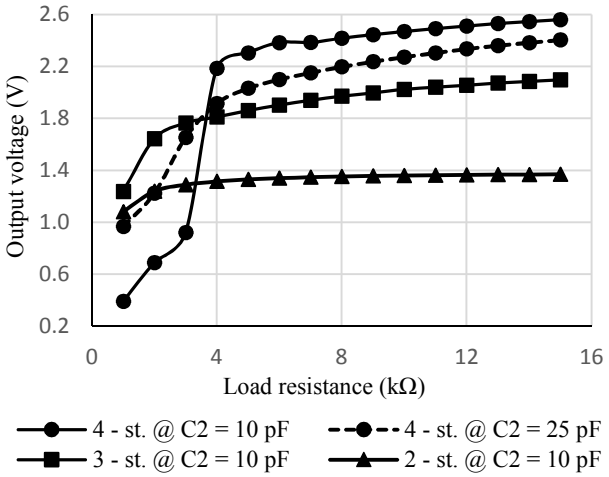

Fig. 6. The variation of DC-DC converter output voltage with the load resistance.

The peak power of the 2-4 stage of the DC-DC converter is > 1 mW as shown in Fig. 7. The 3-stage DC-DC converter can achieve higher peak output power compared to the other stages as it can operate at low load resistance compare to the higher stages. The 2-4 stages DC-DC converter have the peak efficiency of 43%, 40% and 34% at 0.2 input as illustrated in Fig. 8. The increase of secondary LC tank capacitor leads to decrease the output characteristics of the DC-DC converter due to the increase of power consumption and partial discharge during the charging and discharging process. The proposed DC-DC converter can self-started from the input voltage of 60 mV and boost into > 500 mV as illustrated in Fig. 9 for a parallel load of 1 MΩ and 10 pF. The voltage quadrupling LC tank connected DC-DC converter with > 8-stages can achieve > 1.0 V for > 70 mV input at >1 MΩ load resistance.

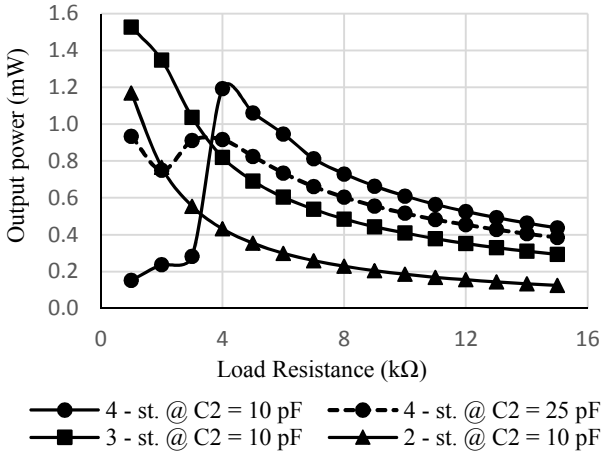

Fig. 7. The variation of DC-DC converter output power with the load resistance.

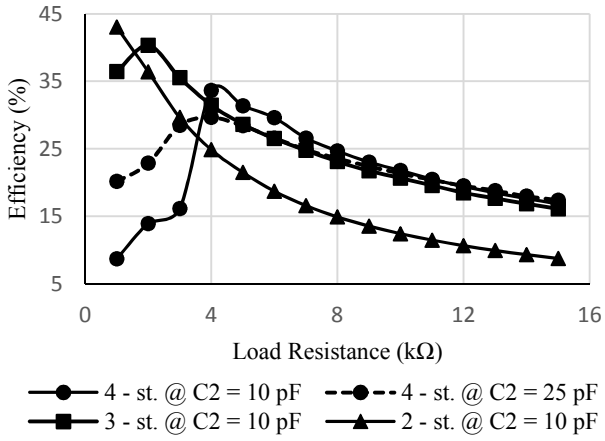

Fig. 8. The variation of DC-DC converter efficiency with the load resistance.

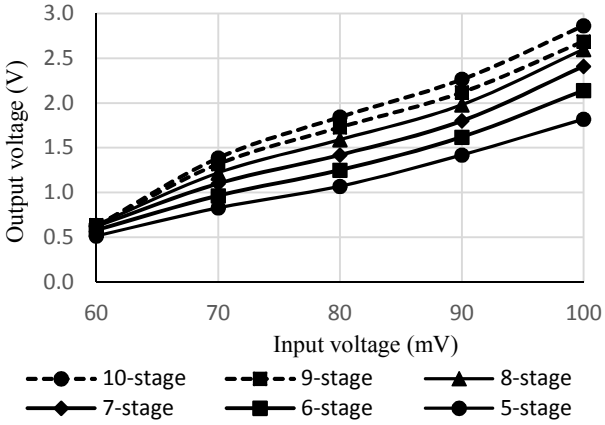

Fig. 9. The variation of DC-DC converter output voltage with input voltage for different stages at 1 MΩ load resistance and 10 pF load capacitance.

Table 1. Comparison with fully integrated ultra-low voltage DC-DC converters in literature.

Ref.	Proc (nm)	Min. input (mV)	Output voltage (V)	Output power (μW)	Peak efficiency (%)	No. of stages
[15]	65	100	1.2 @ 0.14 V input & 1 MΩ load	10@ 0.12 V input	33@ 0.10 V input & 1 MΩ load	-
[16]	130	80	1.0 @ 0.08 V input & 1 MΩ load	1 @ 0.08 V input	24 @ 0.08 V input & 1 MΩ load	10
[17]	180	150	2.1 V @ 0.2 V input & 140 kΩ load	120 @ 0. 20 V input	35@ 0.20 V input & 40 kΩ load	5
[18]	180	110	1.8 V @ 0.2 V input & 15 kΩ load	530 @ 0. 20 V input	46 @ 0.20 V input & 6 kΩ load	5
This work	180	60	2.56 V @ 0.2 V input & 15 kΩ load	1200 @ 0. 20 V input	34 @ 0.20 V input & 4 kΩ load	4

6. Conclusion

A DC-DC converter with novel fully integrated voltage quadrupling LC tank oscillator has been designed, analyzed, and simulated in 180nm CMOS technology. A half-circuit model is presented for frequency analysis, and verified using simulation results. The multi-stage DC-DC converter topology has been proposed to achieve the desired output for different inputs using corresponding DC-DC converter stages. The minimum start-up voltage of 60 mV is achieved by implementing the voltage quadrupling oscillator. The 2-stage DC-DC converter can yield 1.1 V output and 560 μW load power with 43% peak efficiency at 0.2 V input. The 10-stage can achieve an output of 1.32 V and 4.74 V for 70 mV and 200 mV input respectively at 1 MΩ load. The proposed design has excellent performance in terms of minimum startup, peak output power, output voltage, and efficiency compared to alternative on-die ultra-low voltage DC-DC converters in literature, as illustrated in Table 1.

7. References

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