Tunable Active Front-End Realized by Using Zero-IF Down and Up Converters For to be used in Software Defined Radios

Osman Palamutcuogullari, Umut Güvenç
Beykent University, Istanbul, Turkey, osmanp@beykent.edu.tr
TUBITAK BILGEM YITAL, Kocaeli, Turkey, umut.guvenc@tubitak.gov.tr

***Abstract*–The proposed Tunable Active BPF which is operating within 30-512 MHz band is realized by using theZero-IF active Down and Up converters. The operating frequency of the circuit is adjusted by fixing the frequency of the LO which drives the both converters.The bandwidth of the circuit is adjusted by changing the band-width of the active Base-Band LPF which is placed between the two converters. The circuit behaves as a Low-Noise, Narrow-Band Tuned RF Front-End Amplifier with+17 dB Moderate Gain andHigh Selectivity. The input IIP3 is around 5dBm. A single stage NMOS common-gate balanced amplifier is situated at the input to provide the impedance matching and the sharp selectivity. The voltage-series reactive-capacitive feedback is applied to the first stage in order to raise its input impedance for the purpose of impedance matching at the input port as well as for improving its dynamic range and its bandwidth. Implemented in $0.18\,\mu m$ CMOS process technology, a tunable, band-pass 30-to-512 MHz receiver front-end with achieves a maximum of 3.5 dB NF, +18 dB gain, +3dBm IIP3 across the operating band.**

***Index Terms*: Differential-pair converters, common gate, amplifier,Band-pass filter, Baseband filter, IIP3, high linearity, CMOS, tunable, reactive feedback.**

1-INTRODUCTION

The use of Zero-IF converter circuits in radio frequency integrated circuit (RFIC) receivers eliminates the Image-suppression problem. Therefore, they are generally preferred to their super-heterodyne counterparts [1],[2]. In this work, this type of converters are used to realize a tunable narrow-band active band-pass front-end amplifier structure with high blocker suppression behaviour. The proposed structure exhibits acceptable low NF behaviour (NF<4 dB) and moderate dynamic range (IIP3 >5 dBm) and Trancducer-Gain around +17 dB. The block diagram of the circuit is shown in Fig.1. The proposed circuit consists of cascaded three different stages. A front-end comprised with differential common-gate RF amplifier which is followed by a zero-IF Down-Converter (DC) in differential form. Second stage is the Base-Band Amplifier (BBA) which is decorated with a fourth order PasiveRC-Low-Pass Filter (LPF). The last stage is a Zero-IF Up-Converter (UC) in differential form. The Low-Pass behaviour of the internal passive filter turns out to be a Band-Pass filter characteristic with very sharp selectivity. At the output of the UC a passive reactive negative feedback is applied from the output to the input of the CG amplifier to provide the impedance matching at the input and also reflecting the sharp cut-off behaviour of the passive filter to the input (Q Enhencement). The gain of BBA is kept at certain level to provide sufficient loop gain for the feedback structure.

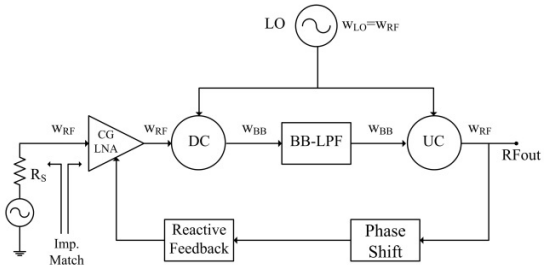

Fig.1. The Block Diagram of the proposed structure.

2-INPUT CG-LNA STAGE

The equivalent circuit of CG-LNAis shown in Fig. 2-1.The DC bias currents of Q_1 and Q_2 are equal $I_{Q1} = I_{Q2}$.

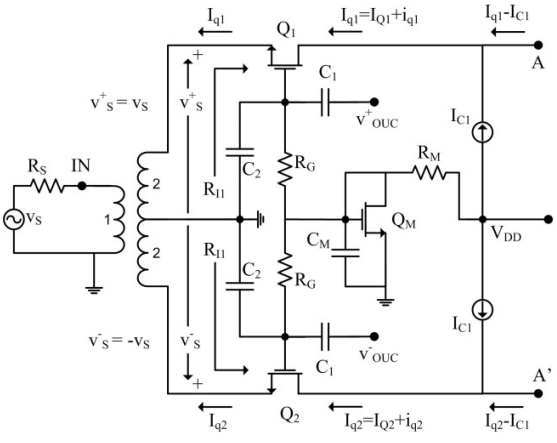

Fig. 2.The equivalent circuit of NMOS CG-LNA.

C_1 and C_2 capacitors are the reactive elements of the voltage-series feedback which is applied from the output to

input to provide impedance matching at the input. The constant current sources $I_{C1} = I_{C2}$ are used in order to keep the bias currents of the Down-Converter transistors small enough to increase its gain and consequently, reduce its NF.

3. ZERO-IF DOWN-CONVERTER(DC) STAGE

The equivalent circuit of the Zero-IF Down-Converter which is realized as Double-Balanced configuration is shown in Fig.3. Considering that $i_{q1} = -(v_S^+ / R_{I1})$ and $i_{q2} = -(v_S^- / R_{I1})$ represent the Small-Signal currents which injected from LNA when the impedance matching is provided at the input, the total Drain currents of the transistors can be written as follows:

$$I_{q1} = I_{Q1} + i_{q1} \; I_{q2} = I_{Q1} + i_{q2} \quad (1)$$

The currents which flow from the common source inputs of the DC transistors become;

$$I_{q1} - I_{C1} = I_{Q1} + i_{q1} - I_{C1}$$

$$I_{q2} - I_{C1} = I_{Q1} + i_{q2} - I_{C1} \, (2)$$

B-B' are the common terminals of DC where the balanced LO signals v_2 and v_2^- are applied.

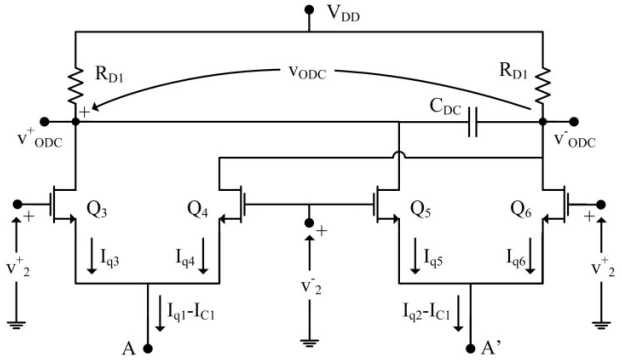

Fig. 3. The equivalent circuit of the Double-Balanced Down-Converter

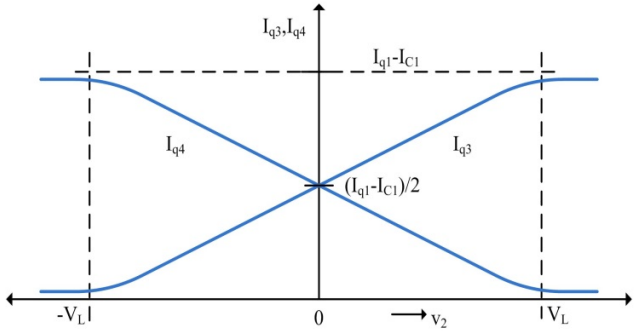

Fig. 4. The drain current variations of NMOS couple in differential form.

The variation of the drain currents of the transistors in Fig. 4 with respect to differential v_2 voltage can be assumed as approximately linear during the transition from conduction to off state[3].With this assumption when the range of LO voltage variation restricted as $|v_2| \le V_L$ the variations of the drain currents can be written as follows:

$$I_{q3} \cong \frac{I_{q1} - I_{C1}}{2}\left(\frac{v_2}{V_L} + 1\right)$$

$$I_{q4} \cong \frac{I_{q1} - I_{C1}}{2}\left(\frac{-v_2}{V_L} + 1\right) \, (3)$$

It can be shown that the edge voltage V_L can be expressed by the following equation[3]:

$$V_L = \sqrt{(I_{Q1} - I_{C1}) / K_{3,4}} \, (4)$$

where, $K_{3,4} = \mu_n C_{OX}\left(\frac{W}{L}\right)_{3,4}$ represent the process parameters of the transistors[1],[2],[3]. When the difference between the currents in (3) is taken and the similar process is applied for the currents of Q_5 and Q_6 v_{ODC} transistors the following results can be obtained.

$$I_{q3} - I_{q4} \cong (I_{q1} - I_{C1}) \times \left(\frac{v_2}{V_L}\right)$$

$$I_{q6} - I_{q5} \cong (I_{q2} - I_{C1}) \times \left(\frac{v_2}{V_L}\right) \, (5)$$

The expression of the small-signal differential output voltage v_{ODC} can be evaluated by using (1) and (2) in (3) as follows:

$$v_{ODC} \cong \left(\frac{v_S^+ - v_S^-}{R_{I1}}\right) \times \left(\frac{v_2}{V_L}\right) \times (R_{D1} // r_{d1}) = 2\frac{v_S}{R_{I1}} \times \left(\frac{v_2}{V_L}\right) \times (R_{D1} // r_{d1}) \quad (6)$$

The expressions for LO may assumed to be a pure sinusoidal voltage in the form of $v_2 = V_O \cos\omega_O t$. The symmetricalRF input source voltages may also be assumed as in the following forms:

$$v_S^+ = V_{RF} \cos\omega_{RF} t \;, \quad v_S^- = -V_{RF} \cos\omega_{RF} t \, .(7)$$

When the last definitions are used in (5) the terms at $(\omega_{RF} \pm \omega_O)$ angular frequencies appear at the output. If the upper side band term is suppressed the by using a simple RC-LPF structure the balanced output voltage of the DC contains only the terms at base-band(BB) spectrum in the form as shown in (8).

$$(v_{ODC})_{BB} \cong \frac{V_{RF}}{R_{I1}} \frac{V_0}{V_L} (R_{D1} // r_{d1}) \cos\omega_{BB} t = (V_{ODC})_{BB} \cos\omega_{BB} t \, (8)$$

Where, $\omega_{BB} = \omega_{RF} - \omega_O$ corresponds to BB angular frequency. The Voltage-Gain is maximum for $V_0 \cong V_L$ and it can be described by a simple expression as follows.

$$A_{V,DC} = \frac{(V_{ODC})_{BB}}{V_{RF}} \cong \frac{(R_{D1} // r_{d1})}{R_{I1}} \quad (9)$$

This result indicates that as long as LO varies within the region where the differential-pair currents exhibits linear variations an DC with a good linear transfer characteristic can be realized. In order to verify the validity of the above analysis the AWR simulation of the circuit is performed by using NMOS transistors with $0.18\mu m$ gate length. The parameters which are usedin the simulation are as follows:

$R_{D1} = 1200\Omega \; r_{d1} \cong 1800\Omega \; (R_{D1} // r_{d1}) \cong 720\Omega$

$R_{I1} = 400\Omega \; I_{Q1} = 21.3mA, \quad I_{C1} = 20.6mA$

$I_{Q1} = 21.3mA \; I_{C1} = 20.6mA \; g_{m1} \cong 50mS$

The Voltage gain is found from (9) as: $A_{V,DC} = 1.8$

The LO Voltageis calculated from (4)as:

$$V_O \le V_L = \sqrt{\frac{I_{Q1} - I_{C1}}{K_{3,4}}} = \sqrt{\frac{21.3 - 20.6}{180.5}} = 62.3mV \cdot$$

$P_{0,AV} \cong -20dBm$

The LO power levels which give the maximum Voltage Gains in the AWR simulations revealed a full compliance with this result.

4. BASE-BAND AMPLIFIER (BBA) STAGE

The circuit is the differential pair where small resistances are added to the source terminals in order improve its linearity as shown in Fig. 5. The terminal DC voltages and the element currents which are used in the circuit simulation are indicated on the figure.

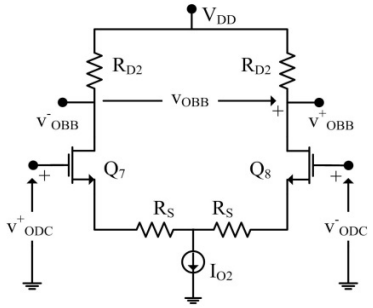

Fig. 5. The Base-Band amplifier in differential form.

The voltage-gain of the circuit can be given as follows.

$$A_{V,BB} = \frac{V_{OBB}}{V_{ODC}} = \frac{(g_m)_{7,8}}{1 + R_S(g_m)_{7,8}}(R_{D2} // r_{d2}) = (G_m)_{7,8}(R_{D2} // r_{d2}) \quad (10)$$

where, $(G_m)_{7,8}$ is the equivalent trans-conductance of the circuit. The parameters which are used in the simulation are as follows:

$K_{7,8} = \mu_n C_{OX}(W/L)_{7,8} \cong 97(mA/V^2)$

$(g_m)_{7,8} = \sqrt{2K_{7,8}(I_{O2}/2)} = \sqrt{K_{7,8}I_{O2}} = \sqrt{97 \times 8{,}5} \cong 29mS$

$$(G_m)_{7,8} = \frac{29}{1 + 20 \times 0{,}029} = 18mS$$

$(R_{D2} // r_{d2}) = (170 // 1200) = 150\Omega$

The Voltage gain is found from (10) as; $A_{V,BB} = 2.7$. The low-pass behaviour of the circuit is provided by adding proper capacitances across the output terminals of DC and BBA. Two more cascaded passive RC Low-Pass stages are included in order to get 4th order Low-Pass characteristic with -24 (dB/octave) Stop-Band slope.

The output of the BBA is applied to the input of a Zero-IF Up-Converter in order to get the original RF signal at its output.

5. ZERO-IF UP- CONVERTER (UC) STAGE

The equivalent circuit of the Zero-IF Up-Converter which is realized as Double-Balanced configuration is shown in Fig.6.

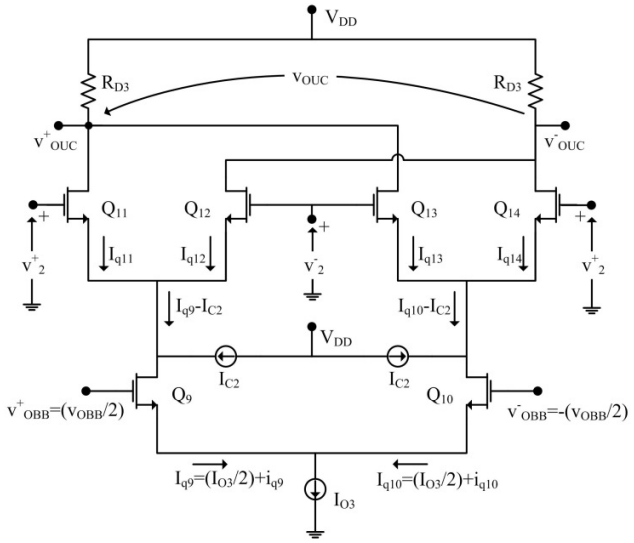

Fig. 6. The equivalent circuit of the Double-Balanced Up-Converter

The structure of the converter is very similar to the circuit which is used as DC. The input is the symmetrical output voltage of the BB amplifier and this voltage is converted to the symmetrical tail currents i_{q9} and $i_{q10}$of the differential pairs. With assumption that LO varies as to keep the differential-pair currents variations within the linear region, the converter output voltagecan be written as follows:

$$v_{OUC} \cong (g_m)_{9,10} \times v_{OBB} \times (\frac{v_2}{V_L}) \times (R_{D3} // r_{d3}) \quad (11)$$

Since,the Voltage-Gain is maximum for $V_0 \cong V_L$ the voltage gain expression of the up-converter turns out to be simple expression as follows:

$$A_{V,UC} = (V_{OUC}/V_{OBB}) \cong \frac{1}{2}(g_m)_{9,10} \times (R_{D3} // r_{d3}) \quad (12)$$

The parameters which are used in the simulation are as follows

$$K_{9,10} = \mu_n C_{OX}(W/L)_{9,10} \cong 105.5(mA/V^2)\ I_{O3} = 25mA$$

$$(g_m)_{9,10} = \sqrt{2K_{9,10}(I_{O3}/2)} = \sqrt{K_{9,10}I_{O3}} = \sqrt{105.5\times 25} \cong 51.4mS$$

$$(R_{D3} // r_{d3}) = (750//1800) \cong 530\Omega$$

Using these parameters in (12) gives the UC voltage gain as:

$$A_{V,UC} \cong \frac{1}{2}(g_m)_{9,10}(R_{D3}/r_{d3}) = \frac{1}{2}51.4\times 0.53 \cong 13.6$$

When the voltage-series feedback is applied from output to input of the half of the differential LNA the input impedance can be written as follows;

$$R_{I1} = R_{IO}(1+\beta A_{VO,1}) \qquad (13)$$

where, R_{I1}, R_{IO}, β, A_{VO1} and $(1+\beta A_{VO,1})$ stand for, input impedance with feedback, input impedance without feedback, return-ratio and return-difference, respectively. Since, 1:4 transformer is used at the input and theinput-impedance without feedback is selected as $R_{IO} = 20\Omega$, the followings can be calculated as;

$$R_{I1} = 400\ \Omega, \quad (1+\beta A_{VO1}) = 20$$

The overall gain of the amplifier without feedback $A_{VO,1}$ is equal to the half of the differential gain without feedback. By using the previously calculated gain values of the individual stages it can be calculated as;

$$A_{VO,1} = \frac{A_{VDC}\times A_{VBB}\times A_{VUC}}{2} \cong \frac{1.8\times 2.7\times 13.6}{2} = 33$$

$$A_{VF,1} = \frac{A_{VO,1}}{(1+\beta A_{VO,1})} \cong \frac{33}{20} = 1.65$$

The total overall gain would be twice as much of this value.

Therefore, $A_{VF,T} = 2\times 1.65 = 3.3 \equiv 10.4dB$

Since, the source and load terminals are the same as $R_S = R_L = 50\Omega$,the overall transducer gain turns out to be:

$$G_T(dB) = A_{V,T}(dB) + 6 = 16.4dB$$

6.SIMULATION RESULTS

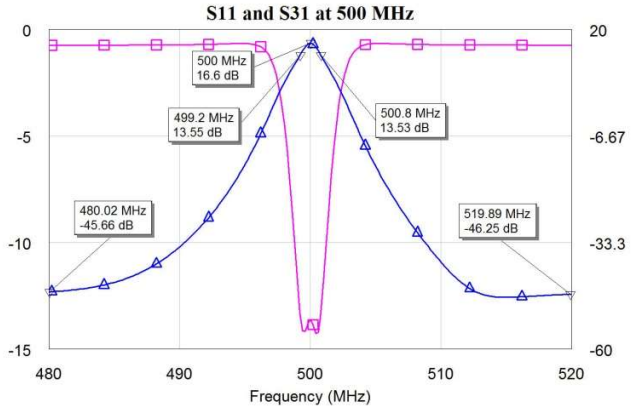

Fig. 7.Input reflection S11 and transducer gain S31 variations at 500MHz.

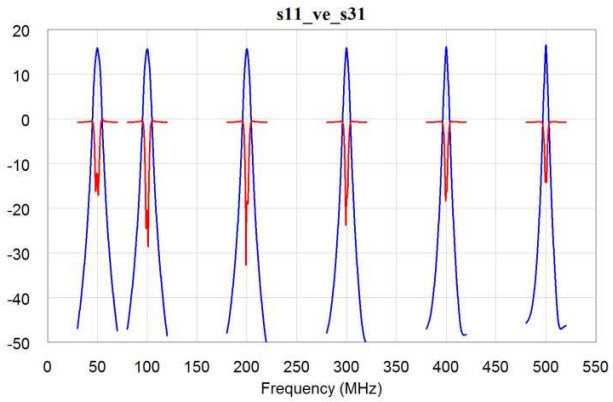

Fig. 8.Shifted frequency responses between 50 - 500 MHz.

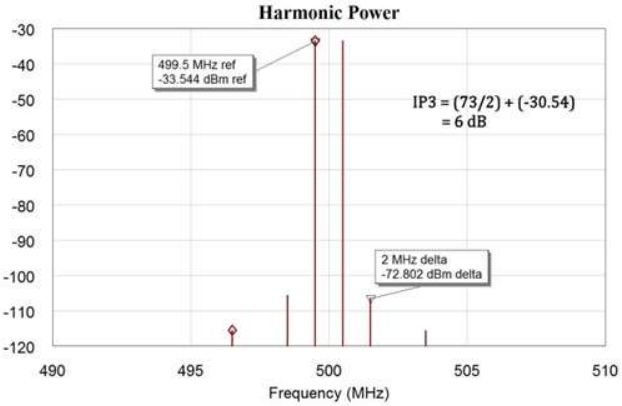

Fig. 9. Two tone test results at 500 MHz.

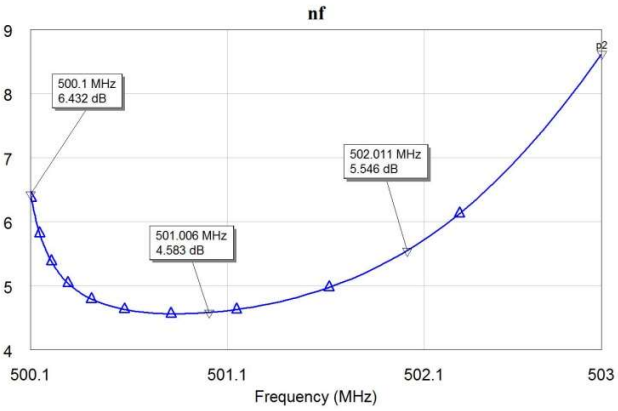

Fig. 10. Noise figure variation within 4 MHz bandwidth at 500 MHz.

6.REFERENCES

[1] B. Razavi, "Design Considerations for Direct-Conversion Receivers", *IEEETrans. Circuits and Systems*, vol.44, pp. 428-435, June 1997.

[2] B. Razavi, "A 900-MHzCMOS Direct-Conversion Receiver."*Dig.ofSymp. On VLSI Circuits,* pp.113-114, June 1997.

[3] J. W. M.Rogers, C. Plett.,Radio Frequency Integrated Circuit Design-Transconductance Controlled Mixer", pp. 240-242, Artech House 2010