New Energy-Aware Evaluation Metric for Compression Circuits

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Abstract

Counter and compressor circuits are key building blocks in digital processing. Much effort has been spent on optimization of individual compression circuits based on traditional performance evaluation metrics, such as compression ratio (C_R). More recently used C_R/Gate-Delay metric reflects compression capability and performance of compression blocks simultaneously, but it does not give an insight into power consumption, which is a vital parameter in contemporary systems with prevailing battery life and power efficiency constraints. This paper proposes a new evaluation measure that incorporates energy consumption: C_R/PDP. This metric is then used to evaluate compression circuits based on simulated power delay product or PDP. Proposed C_R/PDP metric showed that (2,3,3) counter is not as efficient as 4:2 and 5:2 compressor. Similarly, (6,3) and (12,4) are not as efficient as (7,3) and (13,4) respectively when PDP is considered. These properties cannot be detected using the previous C_R/Gate-Delay metric.

1. Introduction

Compression circuits have received interest from the arithmetic processor design groups since 1960's. Multipliers, which are basic arithmetic units in processors, use counters and compressors in their reduction phase. Optimization of compression block size is important in multipliers. Multi-operand addition and digital neural networks are major application domains of counters and compressors in addition to multipliers. It is shown in [1] that 'q' number of counter outputs are presented to the next stage in a conventional (p,q) counter with 'p' number input inputs, given

$$q \geq \log_2 (p+1) . \quad (1)$$

Compressors not only collect 'p' new bits from the previous stage but also 'p-3' carry signals from the right column of the same stage, and bounce the same amount of carries to the left column. For example, (7,3) counter reduces seven bits of same weight into three equivalent bits of different weight for propagation to the next stage, while 4:2 compressors compress four input bits with one carry interchange. If the number of outputs 'q' of the counter in (1) is equal to $\log_2 (p+1)$, then it is known as a saturated counter; otherwise, it is called unsaturated. For instance, (3,2) is a saturated counter, while (4,3) is not a saturated counter. Consequently, if all input bits of a counter have the same weight, it is known as a single column input (SCI) counter, and multiple column input (MCI) counter otherwise.

Compression ratio (C_R), defined as the proportion of input over output bits, is a metric typically used to characterize compression circuits. An alternative metric considers the number of gates in the worst case delay path (WGD) and is referred to as 'C_R/WGD'. 'C_R/WGD' based evaluation covers the theoretical worst delay of counters or compressors. In low activity circuit applications, such as the sensors in IoT applications, power rarely fluctuates. In active systems for data rendering and image processing, power often varies with throughput. Hence, the selection of counters and compressors based on compression ratio or 'C_R/WGD' does not fully serve the purpose of optimizing power dissipation or energy. This paper therefore proposes another metric, 'C_R/PDP', which represents not only the worst delay of the compression block but also the power consumed by it.

In this paper, SCI and MCI, saturated and unsaturated counter and compressor circuits are discussed and compared using existing (C_R/WGD) and proposed (C_R/PDP) evaluation metrics. Section 2 outlines SCI and MCI counters under study. SCI includes saturated (3,2), (7,3) and (15,4) counters and unsaturated counters sandwiched between these saturated counters, whereas MCI includes (2,3,3), (5,5,4) and (3,2,2,2,5) counters. In Section 3, 4:2, 5:2 and 6:2 compressors are described with associated configuration tables and characteristic equations. The comparison for all of the above-mentioned compression blocks is presented in Section 4, with existing and improved comparison matrix. Section 5 concludes the paper.

2. Counter Circuits

2.1. SCI Counter circuits

The (3,2) counter is one of the most widely discussed circuits in the literature and is also known as the Full adder [2], [3]. The (3,2) counter depicted in Fig. 1 was proposed by N. Ohkubo et al.[4]. It has two XORs and one multiplexer (MUX).

P. J. Song et al. [5] proposed the (7,3) counter depicted in Fig. 2, in order to investigate the concept of using a small counter to construct wide counters. Contrary to (3,2), gate delays of (7,3) counter vary w.r.t. output, i.e. 2^0 has four gate delays while 2^1 and 2^2 have six gate delays. A similar approach was taken in [6] to compose the (15,4) saturated counter. The (15,4) counter circuit has six gate delays for 2^0, eight gate delays for 2^1, and ten gate delays for 2^2 and 2^3 outputs.

For SCI saturated 'n' bit counter, general recursive equations (2) and (3) allow calculation of the number of stages and worst gate delay for the n-bit saturated counter.

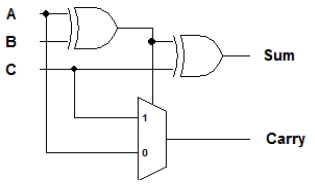


Fig. 1. (3,2) counter circuit or Full Adder [15].

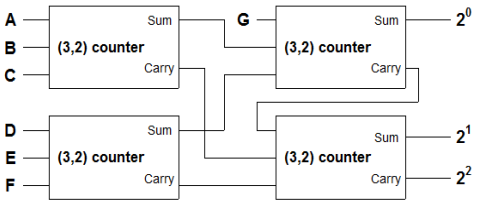


Fig. 2. (7,3) counter circuit.

$$\text{No. of stages} = S = \log_2 (n+1) - 1 \quad (2)$$

$$\text{Worst gate delay} = 2 + 4*\log_2 (n+1) - 1 \quad (3)$$

SCI unsaturated counters are not very common in the literature due to their smaller compression ratio compared to saturated counters with nearly same average power. Unsaturated SCI counters proposed by A. Dandapat [7] have been considered for this study. Typical a half adder structure or a (2,2) counter is deployed in unsaturated counters, which does not help in compression by itself (C_R=1), The (2,2) counter is depicted in Fig. 3. For brevity, only (4,3) unsaturated counter has been shown in Fig. 4, having three (2,2) and one (3,2) counters.

2.2. MCI Counter circuits

Multiple column input counters absorb bits of different weight. The leftmost number in the nomenclature of MCI counters denotes the number of input bits from the most significant column followed by least significant column, whereas the number of outputs is at the rightmost position. (2,3,3) is an example of such an MCI counter, introduced by O. Kwon et al. [10]. (2,3,3) MCI counter compresses five bits with an equivalent weight of seven; three bits of weight 2^n, similar to (3,2) counter, and two more bits of $(n+1)^{th}$ column as depicted in Fig. 5. Irregularity is its drawback, but one can place this counter in parallelogram structures of compression trees, where a SCI counter cannot be placed. Another MCI saturated counter is (2,2,2,3,5) counter. This counter is an extension of (2,3,3) counter, in which two bits of two more columns from left have also been incorporated. This counter has eight gate delays in its worst path and compresses 31 equivalent bit weight of 2^0. Similarly, authors in [11] proposed (5,5,4) MCI counter (later discussed by [12]) which compresses five bits with weight 'n' and five bits with weight 'n+1', as depicted in Fig. 6. (5,5,4) counter has eight gate delays in the worst path with equivalent 15 bits of 2^0 weight.

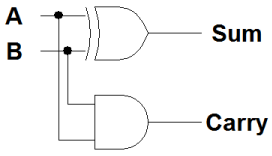


Fig. 3. (2,2) counter or half adder circuit.

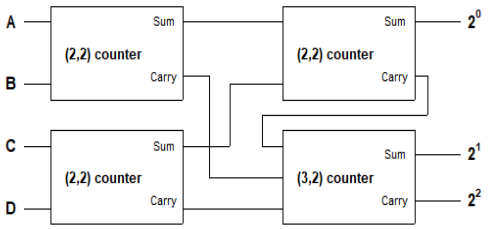


Fig. 4. (4,3) counter

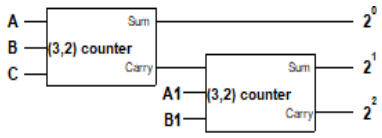


Fig. 5. (2,3,3) counter circuit.

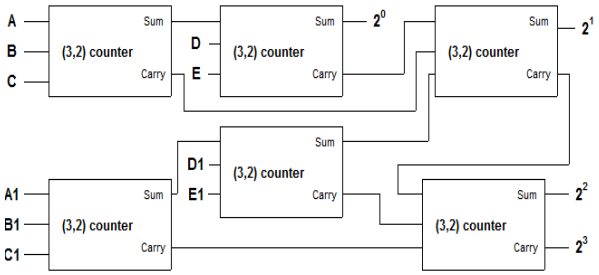


Fig. 6. (5,5,4) counter.

Since regularity is desirable in compression tree of multipliers, an MCI counter with the same input column height is appropriate for compressing parallel bits. Table 1 summarizes the configuration of counter circuits discussed so far. The input to output ratio or Compression ratio (C_R) and worst gate delay have been included in the table. Contrary to SCI saturated counters, the number of AND gates fluctuates with respect to the

Table 1. Configuration Logic Blocks

Counter Size	Number of Stages	Comp. Ratio (C_R)	XOR / MUX gates	AND gates	Worst path gate delays
SCI Saturated Counters					
(3,2)	1	1.50	3	0	2
(7,3)	2	2.33	12	0	6
(15,4)	3	3.75	33	0	10
SCI Un-Saturated Counters					
(4,3)	2	1.33	6	3	9
(5,3)	2	1.67	8	2	10
(6,3)	2	2.00	10	1	11
(8,4)	3	2.00	19	7	26
(9,4)	3	2.25	21	6	27
(10,4)	3	2.50	23	5	28
(11,4)	3	2.75	25	4	29
(12,4)	3	3.00	27	3	30
(13,4)	3	3.25	29	2	31
(14,4)	3	3.50	31	1	32
MCI Saturated Counters					
(2,3,3)	2	1.66	8	0	4
(5,5,4)	3	2.50	18	0	8
(2,2,2,3,5)	2	1.80	12	0	8

counters, the number of AND gates fluctuate with respect to the position of the counter. If an unsaturated counter is followed by a saturated counter, then it has the most number of AND gates, which is undesirable, and vice versa for an unsaturated counter following a saturated counter. This effect is notable in (6,3) and (8,3) SCI unsaturated counter.

3. Compressor circuits

Compressor circuits allow the horizontal flow of bits by means of carries, in parallel with the vertical flow. A simple illustration of 4:2 compressor contains pair of cascaded (3,2) counters [5], having the worst path of four XOR gates. This delay is further optimized in [4] to three gate delays by dissolving cell hierarchy into one single unit, although the total number of gates is retained in the optimized structure (Fig. 7). Due to its flexibility of propagating carries in horizontal and vertical directions, the 4:2 compressor is commonly used as a building block for wide compressors, such as 6:2 and 9:2. The 5:2 compressor process five new bits and two carries from adjacent columns. Similar to 4:2 compressors, it can be realized with three full-adder circuits, having worst case delay of six XOR/MUX gates. This structure of 5:2 compressor was optimized in [13] to four gate delays, as depicted in Fig. 8. Similarly, 6:2 compressor circuit based on the 4:2 compressor is shown in Fig. 9. Table 2 depicts the configuration of compressor circuits. It is evident from Table 2 that the growth of the number of gates, compression ratio (C_R) and worst gate delay is linear with the compressor size.

4. Comparison of Counters and Compressors

Evaluating compression circuits based on only compression ratio (C_R) is not meaningful since compression circuits have different gate delays in the worst path. A compression circuit can have a high compression ratio with poor performance. For this reason, V. G. Oklobdzija [1] introduces 'C_R/WGD', which categorizes compression circuits based on a number of gates in the worst path. For example (7,3) counter has C_R = 2.33 (7/3), with six XOR or MUX gates in the longest path. Thus, C_R/WGD

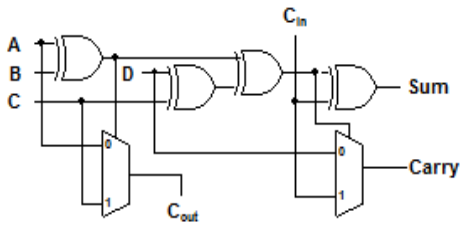


Fig. 7. 4:2 compressors.

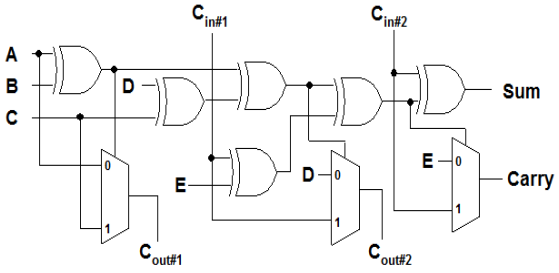


Fig. 8. 5:2 compressors.

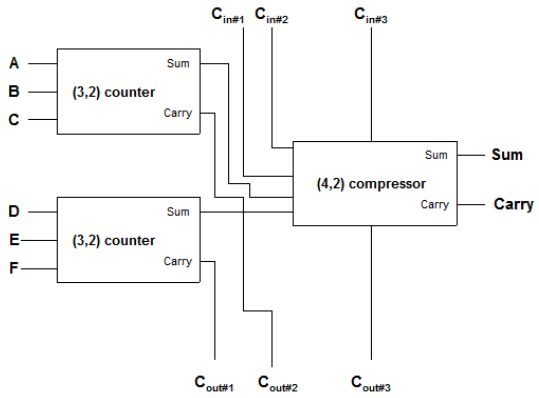


Fig. 9. 6:2 compressors.

Table 2. Configuration of compressors

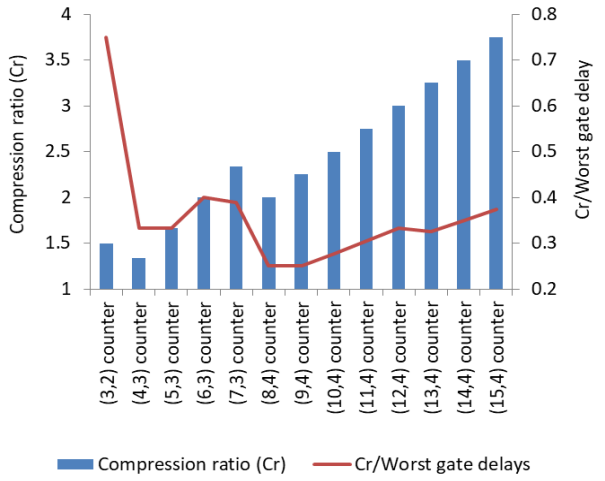
	XOR / MUX gates	Comp. Ratio (C_R)	Worst Path Gate Delays
4:2 Compressor	6	2	3
5:2 Compressor	9	2.5	4
6:2 Compressor	12	3	5

= 0.388 (2.33/6). C_R and C_R/WGD scores of counters and compressors discussed thus far are depicted in Fig. 10. As shown, gate delays vary with input bits. After SCI saturated counters (3,2) and (7,3) in Fig. 10.a., C_R drops and increases linearly. C_R/WGD, on the other hand, drastically drops after saturated SCI counters and roughly increases in a linear manner afterward. Similarly, a linear decay in C_R/WGD can be observed in Fig.10.b. as MCI counter and compressor size increases.

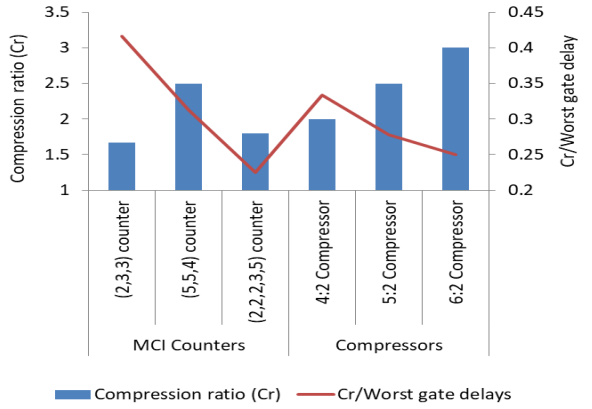
R. Zimmermann et al. [9] perform detailed logic style comparison, and conclude that for arbitrary combinational circuits, static complementary CMOS logic outperforms other styles in every aspect, whereas for complex gates like XOR and multiplexer or MUX, the pass transistor logic family is better. To calculate the actual PDP of compression blocks for the proposed metric in this study, dual pass logic (DPL) has been used for circuit realization. DPL style introduced by M. Suzuki et al. [8] has a relatively high average current, but PDP is low compared to other logic styles. For a fair PDP calculation, two loading scenarios have been designed to stress the compression circuits systematically through all possible input vectors: a) When the most active bit is the most significant bit (MSB), and b) when the most active bit is the least significant bit (LSB).

All simulations in this study are completed using Cadence tool in 180nm technology. Supply voltage and temperature represent nominal condition at 1.8 V and 27˚C respectively. The edge rate of all inputs is 20ps/V with most active input switching at a rate close to system maximum frequency limit i.e. 250 MHz. To provide more realistic slew rates, two unit buffers have been installed at inputs while every output of compression circuit under test has been loaded with 5 fF of capacitance. C_R and C_R/PDP of SCI counter circuits are depicted in Fig. 11.

Ideally, a counter has maximum C_R with minimum PDP. Similar to C_R/WGD in Fig. 10.a., C_R/PDP also drops in Fig. 11 for large counters. However, C_R/PDP recovers more linearly to next SCI saturated counter compared to C_R/WGD. For instance, C_R/WGD indicates that saturated (7,3) counter has poorer performance than (6,3) unsaturated counter, which is corrected



a. SCI counters



b. MCI Counters and Compressors

Fig.10. Compression ratio (C_r) and C_r/WGD of compression block.

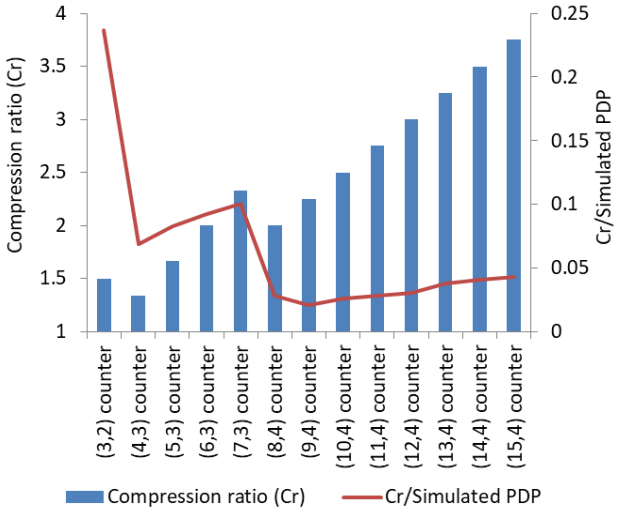


Fig. 11. Compression ratio (C_r) and C_r/PDP of SCI saturated and unsaturated counters **.**

by C_R/PDP in Fig. 11. Same is the case with (12,4) and (13,4) counters. Furthermore (5,4) is more efficient in terms of C_R/PDP compared to (4,3) unsaturated counters. C_R/PDP drops further after saturated (7,3) counter, but it recovers gradually compared to the trend following (7,3) counter. This trend indicates PDP improves more rapidly from saturated (3,2) to (7,3) counters compared to (7,3) to (15,4) saturated counters. This can be explained by examining the number of AND gates used in SCI unsaturated counters.

Use of AND gate is not desirable for counter DPL circuits, because one input of AND gate is connected to either ground or supply permanently, which creates a path for short circuit current. Fig. 12 depicts the number of AND gates in SCI unsaturated counter circuit. For the unsaturated counter, XOR or MUX gate number linearly varies, while AND gates abruptly go to maximum for unsaturated counter followed by the saturated counter. For small counters (smaller than (7,3) counter), the effect of short circuit current dominates, so C_R/PDP grows linearly with the linear decrease in AND gates. In large counters (larger than (7,3) counter), the number of XOR or MUX gates are high enough such that activity of node capacitance dominates the short-circuit current and PDP shows the intermediate effect of both activity and short circuit currents.

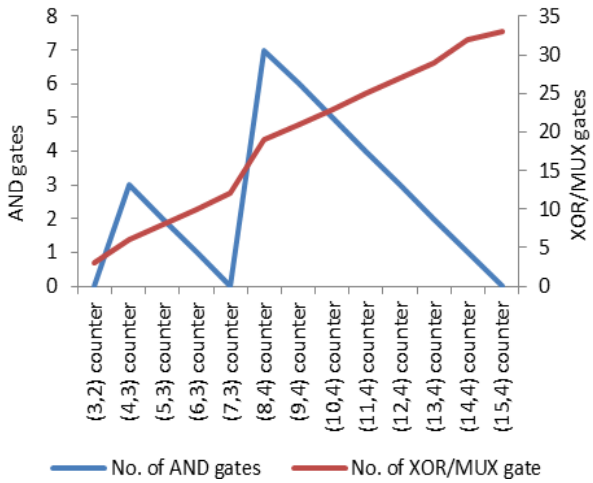


Fig. 12. Logic gates used in SCI saturated and unsaturated counter circuits.

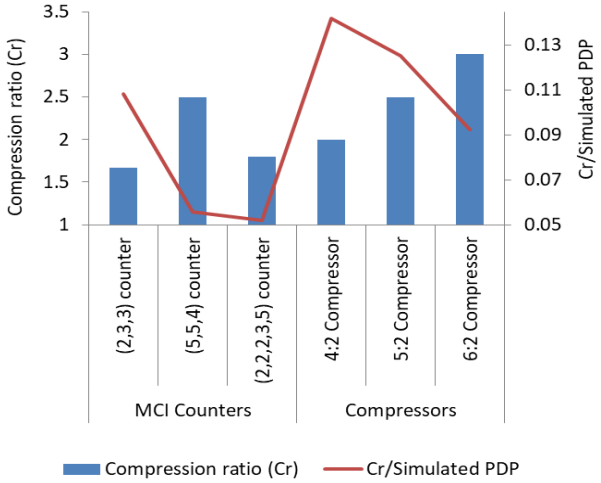


Fig. 13. Compression ratio (C_r) and C_r/PDP of saturated and unsaturated SCI counters.

Fig. 10.a. indicates that wider saturated counters like (15,4) will perform equally well in C_R/WGD as saturated (7,3) counters, while simulation results of PDP show that wider saturated counters have a relatively high PDP penalty for the delivered compression ratio. Fig. 13 depicts the C_R/PDP of MCI counter and compressor circuits. If only C_R/WGD based evaluation in Fig.10.b is considered, MCI saturated (2,3,3) counter is the best option in MCI counters and compressors, while C_R/PDP metric in Fig. 13 reveals that 4:2 and 5:2 compressors are more efficient than (2,3,3) counter for targeting energy-aware systems. While C_R/WGD decreases linearly, a sharp decrease in C_R/PDP can be observed in MCI counters.

4. Conclusion

In this paper different types of SCI, MCI saturated and unsaturated counters and compressors have been discussed and compared based on existing and proposed metrics. Proposed metric, C_R/PDP, provides a method to evaluate power as well as the actual delay of a compression block. The trends observed from the new metric revise the assumptions based on existing metrics. Proposed metric also helps to objectively forecast effectiveness of wider counters and compressors. The general contribution of the proposed metric, i.e. the observation that wider saturated counters and compressors perform worse than smaller saturated counters and compressors in energy aware applications, helps the designer compare and choose the most appropriate compression block for different applications.

5. References

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