CMOS Current Mode Exponential Function Generator Circuit Using Pade Approximation

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***Abstract*—This paper presents a new exponential function approximation, using Pade approximations. An exponential function generator circuit is designed in CMOS 0.35µm technology using the proposed approximation methodology. Its performance is measured to verify the mathematical analysis using SPICE tool. The results verified that Pade approximation equations can be used in design of EXPFGs and with a judicious choice of the numerator and denominator polynomials, substantial improvement in the dynamic range can be achieved without having to sacrifice circuit complexity.**

Keywords—exponential function generator, CMOS design, Variable Gain Amplifier

I. INTRODUCTION

Over the past few years, the importance of high-speed wireless communication becomes greater and greater due to the high demand of more powerful mobile devices [1]. Automatic Gain Control (AGC) circuits including Variable Gain Amplifiers (VGA) are acting an important role as a building block of wireless communication systems by providing fixed output power for different levels of input signal. This characteristic increases the dynamic range of the entire system [2]. The VGAs are widely used in communication systems such as the Wideband Code-Division Multiple Access (WCDMA) wireless communication systems [3], CDMAs [4], wireless sensor networks (WSN) [5], Adaptive Antenna Combining (AAC) systems [6], Wireless Personal Area Networks (WPAN), Portable communication drivers [7], and direct-conversion receivers [8]. The VGAs also play important role in biomedical signal acquisition [9], medical equipment [10], hearing aids [11], imaging [12], disk drives [13] and audio/video analogue signal processing circuits [14].

VGAs can be classified according to their control function. The control function can be an analogue (continuous) signal or a discrete signal. The VGAs that are controlled with continuous signal are either controlled with a linear signal or an exponential signal. Exponential control signals are preferred because of their higher dynamic range characteristics. To realize exponential signals, devices with exponential DC characteristics can be used. Whilst CMOS technology lacks devices that have exponential characteristics in linear or saturation regions, exponential function approximations are used as the functions that will be realized with MOSFET devices working in saturation region.

In this paper, a new exponential function approximation, using Pade approximations is proposed. Pade approximation is preferred because it provides a better result compared to most common approximation method, Taylor series approximation with the same order. An exponential function generator circuitis designed using the proposed approximation methodology in CMOS 0.35µm technology, under supply voltage of 3.3V. Its performance is measured to verify the mathematical analysis using SPICE tool. The results verified that Pade approximation equations can be used in design of EXPFGs and a proper order of numerator and denominator can be selected according the specifications of the VGA.

II. THE PROPOSED APPROXIMATION FUNCTION

A. Pade Approximation

Recently, it is observed that there is connection between some Pade approximants and ideal exponential function [15].

When the Pade table is constructed for the exponential series given in (1), the equations given in Table1 are established to represent the function given in (2) [16].

$$e^{ax} = 1 + \frac{ax}{1!} + \frac{m,na^2x^2}{2!} + \cdots + \frac{a^n x^n}{n!} + \cdots \quad (1)$$

$$P_{m,n}(x) = \frac{n_m(x)}{d_n(x)} \quad (2)$$

Comparison of Taylor series approximation and Pade approximation is given in Figure 1. Here the order of the Taylor series approximation function n equals to 2 and the order of Pade approximation's numerator and denominator m and n are also equal to 2. For the same order of equations, it is obvious that Pade approximation is more accurate for a larger interval.

TABLE I. A PORTION OF PADE TABLE FOR e^x

$m\backslash n$	0	1	2	3
0	$\frac{1}{1}$	$\frac{1}{1-x}$	$\frac{1}{1-x+\frac{1}{2}x^2}$	$\frac{1}{1-x+\frac{1}{2}x^2-\frac{1}{6}x^3}$
1	$\frac{1+x}{1}$	$\frac{1+\frac{1}{2}x}{1-\frac{1}{2}x}$	$\frac{1+\frac{1}{3}x}{1-\frac{2}{3}x+\frac{1}{6}x^2}$	$\frac{1+\frac{1}{4}x}{1-\frac{3}{4}x+\frac{1}{4}x^2-\frac{1}{24}x^3}$
2	$\frac{1+x+\frac{1}{2}x^2}{1}$	$\frac{1+\frac{2}{3}x+\frac{1}{6}x^2}{1-\frac{1}{3}x}$	$\frac{1+\frac{1}{2}x+\frac{1}{12}x^2}{1-\frac{1}{2}x+\frac{1}{12}x^2}$	$\frac{1+\frac{2}{5}x+\frac{1}{20}x^2}{1-\frac{3}{5}x+\frac{1}{20}x^2-\frac{1}{60}x^3}$
3	$\frac{1-x+\frac{1}{2}x^2-\frac{1}{6}x^3}{1}$	$\frac{1+\frac{3}{4}x+\frac{1}{4}x^2+\frac{1}{24}x^3}{1-\frac{1}{4}x}$	$\frac{1+\frac{3}{5}x+\frac{1}{20}x^2+\frac{1}{60}x^3}{1-\frac{2}{5}x+\frac{1}{20}x^2}$	$\frac{1+\frac{1}{2}x+\frac{1}{10}x^2+\frac{1}{120}x^3}{1-\frac{1}{2}x+\frac{1}{10}x^2-\frac{1}{120}x^3}$

In order to obtain an improved performance, an immediate approach is to increase the order of the Taylor approximation. However, in case the order is set to 3 or higher, the corresponding circuit requires building blocks realizing x^3 terms whichcan be usually realized using complicated circuitry compared to x^2 or x^4 terms. This is because the voltage-current transfer characteristic of the MOSFET obeys the square-law characteristic, thus CMOS circuits have simpler circuit implementation of x^2 and x^4 terms. Hence, very effective and high-performance squarer circuits are already presentedin the literature. On the other hand, asshown in Figure 2, the rational Pade functions of second-orderprovides similar or better error performance compared to third order Taylor approximation. This is the main motivation of using Pade approximations in the realization of the exponential function generator.

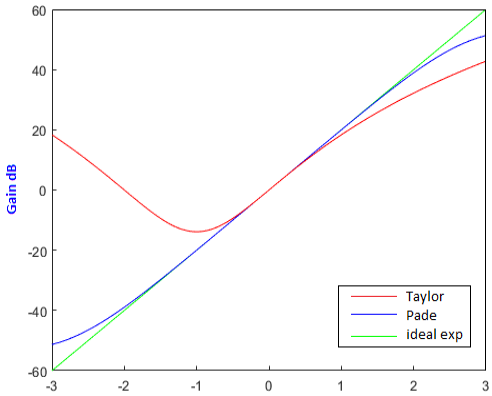

Fig. 1. Comparison of Taylor series approximation and Pade approximation.

It can be argued that the rational form of the Pade function complicated the design, which in fact is not true. This is because in the any multiplier block, input-output characteristic is inherently of rational form, e.g. for current-mode multipliers:

$$I_{out} = \frac{I_x I_y}{I_0} \tag{3}$$

Therefore, it can be thought that the general rational form of Pade approximation does not implies any difficulties in circuit implementation.

Considering all the above discussion, in this thesis work, instead of using a higher order Taylor series approximation, Pade approximation is preferred as the base approximation function.

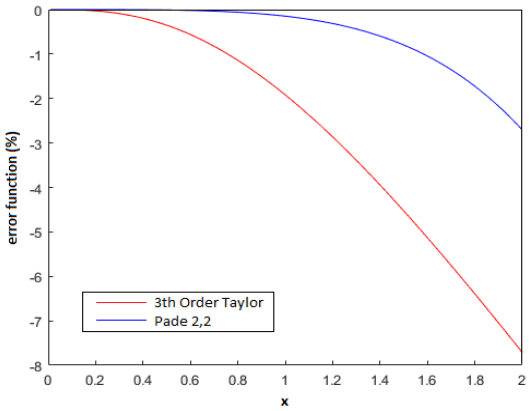

Fig. 2. Error function of Taylor series approximation and Pade approximation.

B. *Proposed Exponential Function Approximation Using Pade Approximation*

A combination of pseudo-Taylor approximation, where $e^x = e^{0.5x}/e^{-0.5x}$, and Pade approximation is proposed in this paper and the equation is modified as below.

$$e^x = \sqrt{e^x}\sqrt{e^x} \tag{4}$$

Using MATLAB for calculations, it is found out that instead of using the same Pade function e.g. $Pade_{2,2}$ twice in (4), using conjugate pairs gives better result. Table 2 shows the input ranges of the Pade approximation for different m and n values.

TABLE II. INPUT RANGES OF PADE FUNCTIONS

$P_{m,n}$ x $P_{m,n}$	Function	Input Range
$P_{0,2}$ x $P_{0,2}$	$\frac{8}{8-4x+x^2}\cdot\frac{8}{8-4x+x^2}$	±0.99

$P_{m,n}$ x $P_{m,n}$	Function	Input Range
$P_{1,1}$ x $P_{1,1}$	$\frac{4+x}{4-x}.\frac{4+x}{4-x}$	±1.36
$P_{1,2}$ x $P_{1,2}$	$\frac{24+4x}{24-8x+x^2}.\frac{24+4x}{24-8x+x^2}$	±2.2
$P_{2,0}$ x $P_{2,0}$	$\frac{8+4x+x^2}{8}.\frac{8+4x+x^2}{8}$	±0.99
$P_{2,1}$ x $P_{2,1}$	$\frac{24+8x+x^2}{24-4x}.\frac{24+8x+x^2}{24-4x}$	±2.2
.$P_{2,2}$x $P_{2,2}$	$\frac{48+12x+x^2}{48-12x+x^2}.\frac{48+12x+x^2}{48-12x+x^2}$	±3.551
$P_{0,2}$ x $P_{2,0}$	$\frac{8}{8-4x+x^2}.\frac{8+4x+x^2}{8}$	±1.1
$P_{2,1}$ x $P_{1,2}$	$\frac{24+8x+x^2}{24-4x}.\frac{24+4x}{24-8x+x^2}$	±3.05

III. EXPFG GENERATOR CIRCUIT USING PADE$_{(2,1)x(1,2)}$

To implement Equation (5), the ratio of input current and the reference current ($x = I_x/I_{ref}$) is used as expansion variable in the system below.

$$e^x = \sqrt{PADE_{2,1}(x)}\sqrt{PADE_{1,2}(x)} \tag{5}$$

The block diagram of the proposed exponential function generator is given in Figure 3.

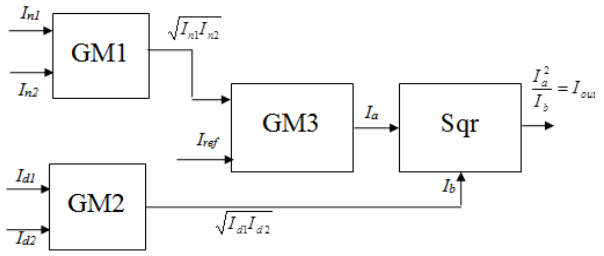

Fig. 3. The proposed exponential function generator.

"GM" blocks represent the 2-input geometric mean circuits and "Sqr" represents a squarer circuit. The output current of the circuit above is given in equation (6), which is the circuit implementation of equation (4).

$$I_{out} = \sqrt{\frac{I_{n1}}{I_{d1}}}\sqrt{\frac{I_{n2}}{I_{d2}}} = \sqrt{\frac{I_{n1}I_{n2}}{I_{d1}I_{d2}}} \tag{6}$$

A. Multiplier/Divider

The current-mode analogue multiplier/divider circuit in [17], which consists of a geometric mean block and a squarer block, is usedfor implementation.Figure 4shows the operation principle of the multiplier/divider circuit.

The input-output characteristic of the multiplier/divider is given below.

$$I_{out} = \frac{I_x I_y}{I_w} \tag{7}$$

This structure is very suitable for this work hence multiple g-mean circuits and a squarer can be used to form the exponential function generator circuit.

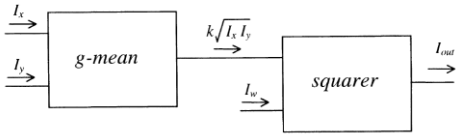

Fig. 4. Principle of multiplier/divider

B. Circuit Realisation

According to the Pade Table PADE$_{1,2}$and PADE$_{2,1}$ functions are given below.

$$PADE_{1,2}(x) = \frac{n_1(x)}{d_1(x)} = \frac{6+2x}{6-4x+x^2} \tag{8}$$

$$PADE_{2,1}(x) = \frac{n_2(x)}{d_2(x)} = \frac{6+4x+x^2}{6-2x} \tag{9}$$

For $x = I_x/I_{ref}$, these equations can be written as (10) and (11), where the coefficients are also divided to 2 for device size considerations.

$$PADE_{1,2}(x) = \frac{I_{n_1}}{I_{d_1}} = \frac{3I_{ref}+I_x}{3I_{ref}-2I_x+\frac{I_x}{2I_{ref}}^2} \tag{10}$$

$$PADE_{2,1}(x) = \frac{I_{n_2}}{I_{d_2}} = \frac{3I_{ref}-I_xI_{ref}+2I_x+\frac{I_x}{2I_{ref}}^2}{3} \tag{11}$$

Using these equations Equation 5 is calculated and given below.

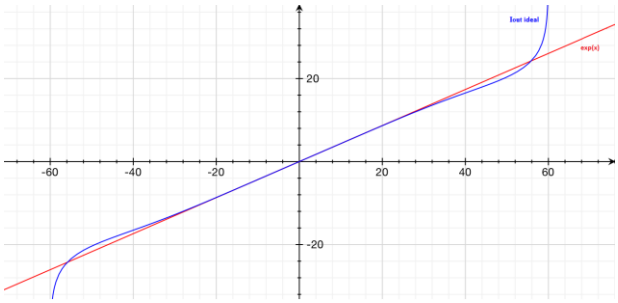

Fig. 5. Calculated output of proposed function

The nominator and denominator functions in Equation 10 and Equation 11 are released by current mirrors and squarer circuits as shown in Figure 6.

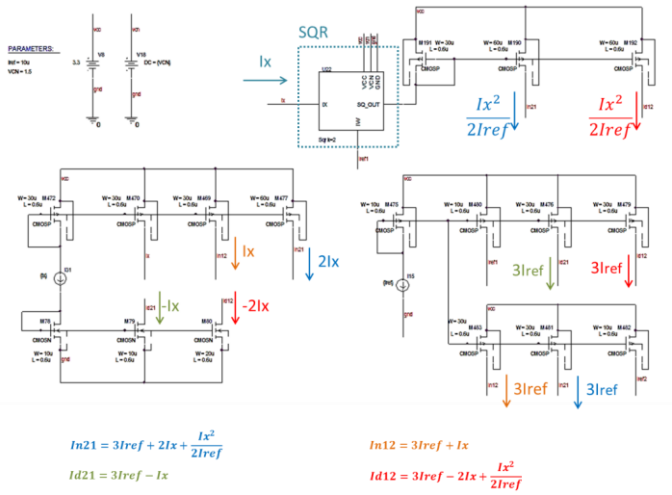

Fig. 6. Current mode circuit realization of n_1, n_2, $d_1$and $d_2$functions.

Circuit realisation of the block diagram is given in Figure 7. Current mirrors are used to change the direction of the output currents of G-mean blocks.

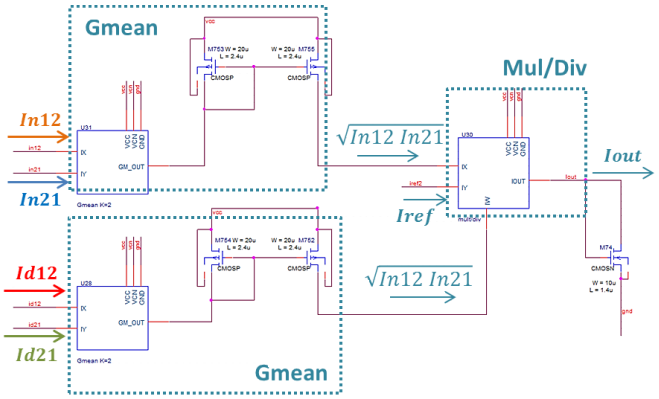

Fig. 7. Current mode circuit realization of n_1, n_2, $d_1$and $d_2$functions.

IV. Simulation ResultS

The circuit is designed in CMOS 0.35µm technology, under supply voltage of 3.3V and using SPICE tool, its performance is measured to verify the mathematical analysis.

The comparison of the ideal exponential function and the gain function of the proposed circuit are shown in Figure 8. SPICE analysis and the MATLAB results are shown to be agreeing within the gain range of -26.3dB to 26.3dB.

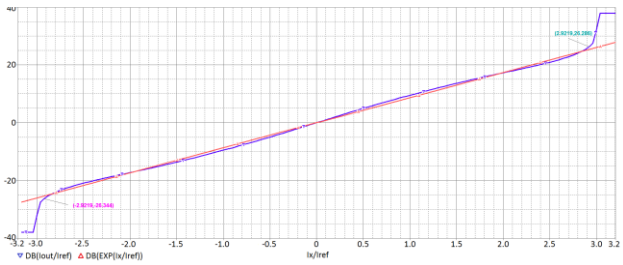

Fig. 8. The comparison of the ideal exponential function and the gain function of the proposed circuit

The error function of the output current is given in Figure 9. It can be seen easily that the error is always less than 1dB within the -2.9 to 2.9 input range. The result is even better than the calculated -2.2 to 2.2 input range

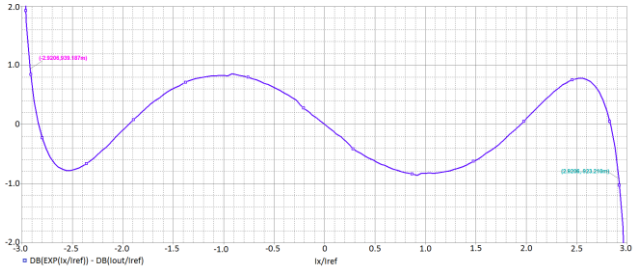

Fig. 9. The error function of the output current.

V. Conclusion

Pade approximation is reported as a new approach forrealizing exponential function in a recent work found in literature, where Taylor series approximation is very common. Using MATLAB for calculations, it is found out that Pade functions of second-order provides similar or better errors performance compared to third order Taylor approximation.A circuit using $PADE_{1,2} \times PADE_{1,2}$ equation is designed with and simulated using SPICE. The proposed circuit has 52.6dB output range, which is a remarkable result for a second order exponential function generator. The output range can also be increased by using Pade functions with higher order of numerator and denominator.

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