# A New Topology for Half-Bridge Z-Source Inverter Based on Gamma Structure

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## Abstract

**In this paper, a new topology for half-bridge Z-source inverter based on Γ-structure is proposed. The proposed inverter can generate higher output voltage in comparison with conventional topologies. In the proposed inverter, not only voltage gain increases by changing the shoot-through duty cycle but also this value increases by changing turn ratio of transformer. Unlike the classic half-bridge inverter, the proposed half-bridge inverter is able to generate zero level in output voltage. In this paper, operation of proposed inverter in different operating mode is presented and design considerations are given. In addition, comparison of boost factor between the proposed and conventional inverters is provided. Finally, simulation results using PSCAD/EMTDC software verifies correct operation of the proposed inverter.**

**Keywords: Half-Bridge, Z-Source Inverter, Gamma Structure**

## 1. Introduction

In recent years, half-bridge and full-bridge Z-source inverters (ZSIs) have been used for increasing the voltage gain. In [1, 2], basic topologies for full-bridge ZSI and quasi-ZSI (QZSI) have been presented. Unlike the ZSI, the QZSI has continuous input current and common ground between input source and inverter stage. In [3], full-bridge series Z-source inverter (SZSI) has been presented. This topology has low voltage stress on capacitors but the value of boost factor is equal to ZSI and QZSI. In order to increase the value of boost factor in SZSI, multiple SZSI has been presented in [4]. This topology uses high number of passive elements in comparison with presented topologies in [1-3]. To reduce number of passive elements in conventional Z-source inverters, switched-boost inverter (SBI) has been presented in [5]. This inverter has lower value of boost factor than ZSI. To resolve discontinuity problem of input current in SBI, current-fed switched inverter (CFSI) has been presented in [6]. In [7], a developed topology for CFSI has been presented. The developed topology uses from several switched-inductors (SL) cells for obtaining high voltage gain. In [8], steady-state analysis and design considerations of switched Z-source inverter have been presented. Although, high voltage gain and continuous input current are important advantages of this topology but number of switches and diodes is high. All presented inverters in [1-8] are full-bridge inverter; however extension of Z-source concept to half-bridge inverters is possible. In [9], a half-bridge Z-source converter has been presented. This topology cannot generate zero voltage level in output. In [10], half-bridge SZSI has been presented. This topology for obtaining high voltage gain uses several impedance networks that cause high size and cost. Unlike the basic topology in [10] which has two impedance networks, the presented half-bridge inverter in [11] has only one impedance network. Boost factor of presented topologies in [10, 11] are not high; hence, half-bridge SBI and quasi-SBI have been presented in [12, 13]. To resolve limitations of SBIs, improved topologies for half-bridge and full-bridge SBI have been presented in [14] that have continuous input current. All presented topologies in [1-14] don't use transformer in their structures but use of transformer can be helpful. In [15-18], transformer-based impedance-source inverters have been presented. In [19-22], improved topologies for trans-Z-source inverters have been presented. To tolerate high voltage by the elements, cascaded topologies for the trans-Z-source inverters have been proposed in [23-26]. In these topologies, instead of using the low number of elements with high voltage-rating, high number of elements with low rating have been used that cause to increase in size, weight and cost.

In this paper, a new Γ-based topology for half-bridge Z-source inverter is proposed. The proposed topology can generate high voltage gain even with low shoot-through duty cycle. In the following, proposed topology is introduced. Then, analysis of the proposed inverter in different operating modes is provided. Next, design considerations are given and the value of critical magnetizing inductance is calculated. Finally, comparison of several topologies and simulation results are provided.

## 2. Proposed Topology

Fig. 1 shows power circuit of proposed topology. According to this figure, the proposed inverter uses two transformers with turn ratio $N_{12} = N_1 / N_2$, diodes $D_1$ and $D_2$, capacitors $C_1$ and $C_2$. Moreover, the proposed half-bridge inverter similar to the classic half-bridge inverter has two switches and two voltage sources. In the proposed inverter, magnetizing inductances of transformers are equal ($L_{m1} = L_{m2} = L_m$) and $C_1 = C_2 = C$.

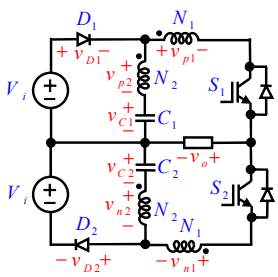



**Fig. 1.** Power circuit of proposed half-bridge inverter

In the proposed inverter, value of voltage across primary winding of upper network ($v_{p1}$) is equal to value of voltage

across primary winding of lower network ($v_{n1}$). Hence, the following equations can be written:

$$v_{p1} = v_{n1} = v_1 \tag{1}$$

$$v_{p2} = v_{n2} = v_2 \tag{2}$$

$$V_{C1} = V_{C2} = V_C \tag{3}$$

$$v_{D1} = v_{D2} = v_D \tag{4}$$

## 2.1. Operating Modes of the Proposed Inverter

As shown in Fig. 2, the proposed inverter has four operating modes. In the first and third operating modes, both switches $S_1$ and $S_2$ are on; so, the proposed inverter is in shoot-through (ST) state. In the second and fourth operating modes, only one of the switches is on; hence, the proposed inverter is in non-ST state.

**First Operating Mode:** In the first operating mode, both switches are on but both diodes are off. By using Kirchhoff's voltage law (KVL) in the upper and lower networks, the following equations can be derived:

$$V_C + v_2 - v_1 - v_o = 0 \tag{5}$$

$$V_C + v_o - v_1 + v_2 = 0 \tag{6}$$

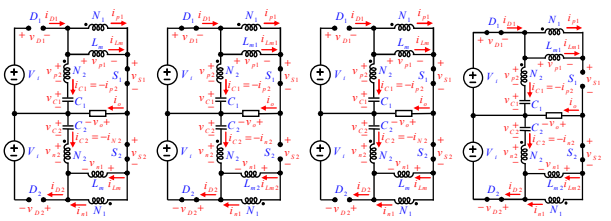
From (5) and (6), average voltage across capacitors and output voltage are calculated as follows:

$$V_C = v_1 - v_2 = \left(1 - \frac{N_2}{N_1}\right) v_1 \tag{7}$$

$$v_o = 0 \tag{8}$$

In this operating mode, voltage across magnetizing inductor $L_m$ is positive; hence, current through it is linearly increased from its minimum value ($I_{L,\min}$) to its maximum value ($I_{L,\max}$). By using (7), current through magnetizing inductor $L_m$ is calculated as follows:

$$i_{Lm} = \frac{v_1}{L_m} t + I_{L,\min} = \frac{N_1 V_C}{(N_1 - N_2) L_m} t + I_{L,\min} \tag{9}$$



(a) (b) (c) (d)

**Fig. 2.** Equivalent circuits of the proposed inverter in different operating modes; (a) First operating mode; (b) Second operating mode; (c) Third operating mode; (d) Fourth operating mode

Since in this operating mode, $i_{p1} = i_{n1} = i_1$ and $i_{p2} = i_{n2} = i_2$; so, by using Kirchhoff's current law (KCL) and $i_2 = \frac{N_1}{N_2} i_1$, the following equations are calculated as follows:

$$i_2 = i_1 + i_{Lm} \tag{10}$$

$$i_{C1} = -i_2 = -\frac{N_1}{N_1 - N_2} i_{Lm} \tag{11}$$

**Second Operating Mode:** In the second operating mode, switches $S_1$ and $S_2$ are on and off, respectively. In addition, both diodes are on. By using KVL, the following equations are written:

$$V_C = V_i - v_2 = V_i - \frac{N_2}{N_1} v_1 \tag{12}$$

$$v_o = v_{o,\max} = V_i - v_1 = V_i - \frac{N_1}{N_2} v_2 \tag{13}$$

In this operating mode, voltage across magnetizing inductor $L_m$ is negative; hence, current through it is linearly decreased from its maximum value ($I_{L,\max}$) to its minimum value ($I_{L,\min}$). By using (12) and KCL, current through magnetizing inductor $L_m$ and other necessary eaquations are calculated as follows:

$$i_{Lm} = \frac{v_1}{L_m} t + I_{L,\max} = \frac{N_1 (V_i - V_C)}{N_2 L_m} t + I_{L,\max} \tag{14}$$

$$i_{p1} + i_{Lm} = \frac{v_{o,\max}}{R} \tag{15}$$

$$i_{C1} = \frac{N_1}{N_2}\left(i_{Lm} - \frac{v_{o,\max}}{R}\right) \tag{16}$$

**Third Operating Mode:** In the third operating mode, both switches are on but both diodes are off. Analysis of proposed inverter in this operating mode is similar to the first operating mode; so for avoiding prolongation, detailed analysis is ignored.

**Fourth Operating Mode:** In the fourth operating mode, switches $S_1$ and $S_2$ are off and on, respectively. In addition, both diodes are on. By using KVL, we have:

$$v_o = v_{o,\min} = -v_{o,\max} = V_i - v_1 \tag{17}$$

Current through capacitor $C_1$ is calculated as follows:

$$i_{C1} = -i_{p2} = -\frac{N_1}{N_2} i_{p1} = \frac{N_1}{N_2} i_{Lm} \tag{18}$$

Fig. 3(a) shows logical diagram and waveforms of switching pattern. Fig. 3(b) shows waveforms of current and voltage in the proposed inverter.

## 2.2. Boost Factor

Average voltage across magnetizing inductor in steady-state is zero; hence, the following equation can be written:

$$\int_0^{T_s} v_1 \, dt = 0 \tag{19}$$

$$\frac{N_1 V_C}{N_1 - N_2} D_{ST} T_s + \frac{N_1 (V_i - V_C)}{N_2} (1 - D_{ST}) T_s = 0 \qquad (20)$$

where $D_{ST}$ and $T_s$ are ST duty cycle and switching period, respectively.

From (20), average voltage across capacitors is calculated as follows:

$$V_C = \frac{(1 - D_{ST})(1 - N_{12})}{1 - N_{12}(1 - D_{ST})} V_i \qquad (21)$$

where allowable interval of ST duty cycle is $0 \le D_{ST} < 1 - \frac{1}{N_{12}}$.

By using (12), (13) and (21), maximum output voltage and boost factor $B = (v_{o,\max} / V_i)$ are calculated as follows:

$$v_{o,\max} = \frac{1 - N_{12}}{1 - N_{12}(1 - D_{ST})} V_i \qquad (22)$$

$$B = \frac{1 - N_{12}}{1 - N_{12}(1 - D_{ST})} \qquad (23)$$

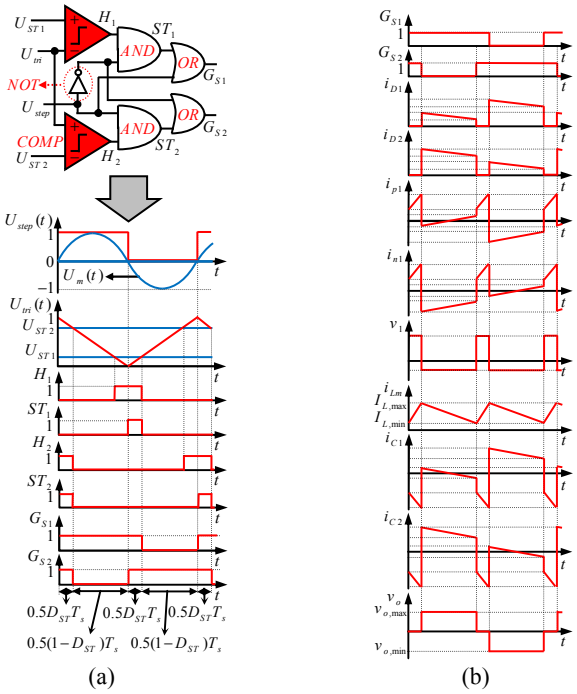



**Fig. 3.** (a) Logical diagram and waveforms of switching pattern; (b) Waveforms of current and voltage

## 3. Design Considerations

Average current through capacitor in steady-state is zero; hence, the following equations can be written:

$$\int_0^{T_s} i_C \, dt = 0 \qquad (24)$$

$$-\frac{N_1}{N_1 - N_2} I_{Lm} D_{ST} + \frac{N_1 (1 - D_{ST})}{2N_2} \left( 2I_{Lm} - \frac{v_{o,\max}}{R} \right) = 0 \qquad (25)$$

By solving (25), average current through magnetizing inductors is calculated as follows:

$$I_{Lm} = \frac{(1 - D_{ST})(N_1 - N_2)}{2R(N_1 - N_2 - N_1 D_{ST})} v_{o,\max} \qquad (26)$$

$$I_{Lm} = \frac{(1 - D_{ST})(N_{12} - 1)^2}{2R[N_{12}(1 - D_{ST}) - 1]^2} V_i \qquad (27)$$

It is important to calculate ripple of current through magnetizing inductors for proper design. By using (7) and (21), the following equations can be written:

$$L_m \frac{\Delta i_{Lm}}{0.5 D_{ST} T_s} = \frac{N_1}{N_1 - N_2} V_C \qquad (28)$$

$$\Delta i_{Lm} = \frac{N_{12} D_{ST} (1 - D_{ST})}{2 L_m f_s [N_{12}(1 - D_{ST}) - 1]} V_i \qquad (29)$$

To calculate voltage ripple across capacitors, $\Delta v_C$, the following equations can be written:

$$` \Delta v_C = \frac{N_1}{N_2 C} \int_0^{0.5(1 - D_{ST}) T_s} \left( \frac{v_1}{L_m} t + I_{L,\max} \right) dt \qquad (30)$$

$$\Delta v_C = \frac{N_{12}(N_{12} - 1)^2 (1 - D_{ST})^2}{4RCf_s [N_{12}(1 - D_{ST}) - 1]^2} V_i \qquad (31)$$

By defining percentage of allowable voltage ripple for capacitors ($x_C\%$) and percentage of allowable current ripple for magnetizing inductors ($x_{Lm}\%$), we have [27]:

$$x_C\% = \frac{\Delta v_C}{V_C} \times 100 \qquad (32)$$

$$x_{Lm}\% = \frac{\Delta i_{Lm}}{I_{Lm}} \times 100 \qquad (33)$$

By substituting (21) and (31) in (32), $x_C\%$ and $C$ are calculated as follows:

$$x_C\% = \frac{N_{12}(N_{12} - 1)(1 - D_{ST})}{4RCf_s [N_{12}(1 - D_{ST}) - 1]} \times 100 \qquad (34)$$

$$C = \frac{N_{12}(N_{12} - 1)(1 - D_{ST})}{4Rx_C\% f_s [N_{12}(1 - D_{ST}) - 1]} \times 100 \qquad (35)$$

By substituting (27) and (29) in (33), $x_{Lm}\%$ and $L_m$ are calculated as follows:

$$x_{Lm}\% = \frac{N_{12} D_{ST} R [N_{12}(1 - D_{ST}) - 1]}{L_m f_s (N_{12} - 1)^2} \times 100 \qquad (36)$$

$$L_m = \frac{N_{12} D_{ST} R [N_{12}(1 - D_{ST}) - 1]}{x_{Lm}\% f_s (N_{12} - 1)^2} \times 100 \qquad (37)$$

It is important to note that calculated inductance from (37) should not result to inappropriate operating states. It is noticeable that there are two operating states in the proposed inverter. In the first operating state, diodes $D_1$ and $D_2$ are turned on and turned off simultaneously and synchronous operation of diodes (SOD) results to four operating modes. These operating modes have been discussed in the previous section. By selecting small magnetizing inductance, synchronous operation of diodes is disrupted. Asynchronous operation of diodes (AOD) in the second operating state results to asymmetrical output voltage with six operating modes. To avoid AOD state, value of magnetizing inductor should be higher than critical inductance ( $L_{m,crit}$ ). In the boundary condition between SOD and AOD, current through diode $D_1$ at the end of the second operating mode is zero. In other words, by using (14) and (16) the following equations can be written:

$$i_{D1} = i_{C1} + i_o = \frac{N_1}{N_2} i_{Lm} - \frac{N_1 v_{o,\max}}{N_2 R} + \frac{v_{o,\max}}{R} = 0 \tag{38}$$

$$L_{m,crit} = \frac{R N_{12}^2 [N_{12}(1-D_{ST})-1] D_{ST}(1-D_{ST})}{2 f_s [2(N_{12}-1)^2 - N_{12}(N_{12}-1)^2(1-D_{ST})]} \tag{39}$$

## 4. Comparison of Boost Factors

In this section, the proposed inverter is compared with conventional topologies in terms of boost factor. Fig. 4(a) shows values of boost factor versus $D_{ST}$ in different values of $N_{12}$ for the proposed inverter. According to this figure, by decreasing the value of $N_{12}$ from 2 to 1, value of boost factor increases. In $N_{12} = 2$, the value of boost factor for the proposed inverter is equal to value of boost factor for conventional ZSI [1]. Fig. 4(b) compares the proposed inverter with conventional topologies when value of $N_{12}$ is $3/2$. Fig. 4(c) compares the proposed inverter with conventional topologies when the value of $N_{12}$ is $4/3$. Fig. 4(d) compares the proposed inverter with conventional topologies when the value of $N_{12}$ is $5/4$. According to Figs. 4(b) to 4(d), the proposed inverter has high boost factor in comparison with conventional topologies.

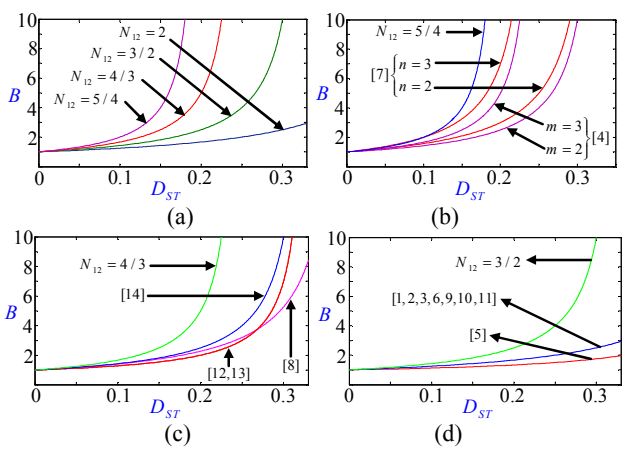



**Fig. 4.** Comparison of boost factors

## 5. Simulation Results

To show correct operation of the proposed inverter, simulation results using the PSCAD/EMTDC software are shown in Fig. 5. Values of used parameters in the simulation are provided in Table 1.

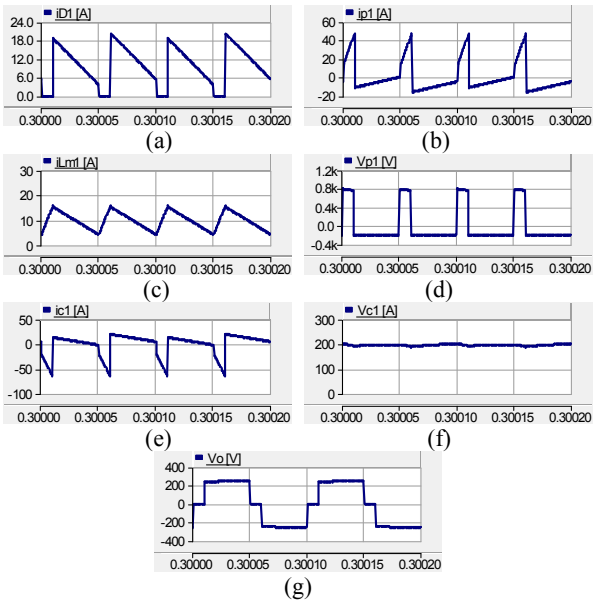



**Fig. 5.** Simulation results in steady-state; (a) $i_{D1}$; (b) $i_{p1}$; (c) $i_{Lm}$; (d) $v_1$; (e) $i_{C1}$; (f) $v_{C1}$; (g) $v_o$

**Table 1.** Values of parameters

| Par. | $V_i$ | $L_m$ | $C$ | $R$ | $N_{12}$ | $f_s$ | $D_{ST}$ |
|---|---|---|---|---|---|---|---|
| Val. | $50V$ | $700\mu H$ | $47\mu F$ | $50\Omega$ | $4/3$ | $10kHz$ | 0.2 |

Fig. 5(a) shows current through diode $D_1$. According to this figure, the diode in ST state is off that is in agreement with theory. Figs. 5(b) and 5(c) show current through primary winding of upper network ( $i_{p1}$ ) and magnetizing inductance, respectively. According to obtained result, average value of current through magnetizing inductance is $9.91A$ that is close to $10A$ calculated from (27). Fig. 5(d) shows voltage across magnetizing inductance. According to this figure, values of voltage in ST and non-ST states are $790V$ and $-196V$, respectively. These values have small differences with calculated values from (7) and (12), respectively. Fig. 5(e) shows waveform of current through capacitor $C_1$. According to this figure, stored energy in capacitor increases in ST state and this energy decreases in non-ST state. Voltage across capacitor $C_1$ is shown in Fig. 5(f). In this figure, average voltage of capacitor is $196V$ that is close to $200V$ calculated from (21). Fig. 5(g) shows voltage across load. According to this figure, output voltage has three positive, negative and zero levels. The values of positive and negative levels are $246V$ and $-246V$, respectively. These values are close to $250V$ and $-250V$ calculated from (13) and (17), respectively. In general,

simulation results have good agreement with obtained results from theory.

## 6. Conclusions

In this paper, a new half-bridge topology for Z-source inverter based on gamma structure was proposed. The proposed inverter uses two transformers for generating higher voltage gain in low values of shoot-through duty cycle. For example, the theoretical value of boost factor for the proposed inverter in $D_{ST} = 0.2$ and $N_{12} = 4/3$ is 5 whereas this value for the conventional ZSI is only 1.67. The proposed inverter has two operating state that were called SOD and AOD states. In the SOD state that proposed inverter has four operating modes, output voltage was symmetric but in the AOD state that proposed inverter has six operating, output voltage is inappropriate. To avoid AOD state, values of critical magnetizing inductances were calculated. Moreover, design considerations and comparison of conventional and proposed topologies were provided. Correct operation of the proposed inverter was verified by simulation results.

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