New Hybrid Quasi Z-source Inverter Based on Diode- Capacitor Basic unit

Sara Laali[1], *Member, IEEE*, Ebrahim Babaei[2], *Senior Member, IEEE,* Vida Ranjbarzad[2]

[1]Faculty of Electrical and Computer Engineering, Islamic Azad University, Tehran North Branch, Tehran, Iran
s.laali@iau-tnb.ac.ir
[2]Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran
e-babaei@tabrizu.ac.ir; vidaranjbarizad@yahoo.com

Abstract

One of the main problems of the Z-source inverters (ZSI) is lack of capability in obtaining high boost factor. In order to recieve this aim, a new hybrid Quasi Z-source inverter (HQZSI) with the capability of obtaining desired boost factor is proposed. The proposed inverter is the combination of diode basic unit and capacitor basic unit as a new basic unit. The one-cell HQZSI is completley analysed and the equations of the diode voltage stress, capacitor votage stress and boost factor are obtained. In addition, it is possible to extend the proposed inverter by increasing the number of used basic units. Two-cell HQZSI and the developed HQZSI that are also analyzed and their related equations are also obtained. Finally, the accuracy performance of the proposed inverter and presented analyses is reconfirmed by using the simulation resluts on the two-cell HQZSI in EMTDC/PSCAD software.

Keywords—Z-source inverter; hybrid QZSI; diode basic unit; capacitor basic unit; boost factor; shoot-through

1. Introduction

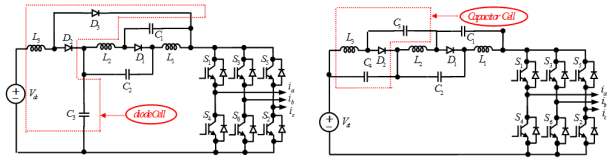
Recently, the Z-source converters (ZSC) have been received more attention in comparison with voltage and current source converters. These converters can acts as dc-dc, dc-ac, ac-dc and ac-ac converter [1-3]. In this paper, the concentration is on Z-source inverter. The first Z-source inverter consists of an X shape inductance which includes of capacitor and inductor [3]. This inverter performs in two operating modes: shoot through (ST) state and non-ST state. Moreover, simple boost, maximum boost and maximum constant boost control methods are three main control methods for ZSIs [4-5].

Up to now, several topologies have been presented for Z-source inverters such as Half-Bridge Switched Boost Inverter [2], Developed embedded switched-Z-source inverter [6], L-Z-source inverter [7], Extended-boost Z-source inverters [8], Switched-Coupled-Inductor Quasi-Z-Source inverter [9] and so on. The main problem of these inverters is their low boost factor. One method to increase the boost factor is increasing the value of duty cycle of ST state. Reducing the value of the modulation index is the main disadvantage of this method. The other way is using additional dc-dc converters that increase the size of inverter, installation space, maintenance and total cost of the inverter [2].

In order to solve this problem a new quasi ZSI is proposed. This new inverter includes of Hybrid basic unit and has the capability to develop to n-cell HQZSI. In section II, firstly the basic QZSI is presented then, the proposed HQZSI is completely analyzed and the equations of the diode voltage stress, capacitor voltage stress and boost factor are obtained. Finally, the correct performance of the proposed HQZSI is reconfirmed through simulation results.

2. Presented topology in [8]

Two topologies of QZSIs that have been presented in [8] are shown in Fig.1. As shown in Fig. 1(a), the conventional ZSI is combined with the diode basic unit to generate diode assisted QZSI. This basic unit consists of two diodes, a capacitor and an inductor to increase the value of boost factor. Moreover, the other QZSI that is shown in Fig 1(b) consists of a capacitor basic unit and a conventional ZSI to obtain higher value of boost factor. These two QZSIs have been investigated and the value of their boost factors and capacitor voltage values have been calculated [8]. In this paper, the other kind of QZSI is proposed that consists of combination of two presented capacitor and diode basic units in [8].



(a) (b)

Fig. 1. Presented QZSIs in [8]; (a) QZSI based on diode basic unit, (b) QZSI based on capacitor unit

3. Proposed HQZSI

In this paper, a new HQZSI based on new hybrid basic unit is proposed. It is possible to develop the proposed inverter by increasing the number of used basic units therefore; one-cell HZSI, two-cell QZSI, three-cell QZSI and finally n-cell QZSI are proposed in this paper. These topologies are completely analyzed in next subsections.

3.1. Proposed one-cell hybrid QZSI

By combination one diode basic unit and one capacitor basic unit, the new hybrid basic unit is generated. The proposed one-cell HQZSI is shown in Fig. 2. As shown in this figure, the new topology consists of one hybrid basic unit with the conventional ZSI. The differ between the conventional ZSI and used ZSI in the proposed topology is the connection of the capacitors C_1, C_2 and inductors L_1 and L_2. According to Fig.2, there is

common earth between the input dc source and inverter part of the topology. This is one of the main advantages of the proposed topology. In addition, the proposed one-cell HQZSI consists of five capacitors, four diodes and four inductors. According to Fig. 2, the inductor L_4 is series-connected to the input dc source that leads to continuous input current to the circuit in this inverter. The conventional control methods that are as same as conventional ZSI are considered in the proposed inverter. The operating modes of this inverter are divided into ST and non-ST states. The inverter can be modelled by a current source and a switch (S). In ST state, the switch of S and diode of D_3 is turned on and the diodes of D_1, D_2 and D_4 are turned off. As a result, the inductors are charged and the capacitors are discharged. In non-ST state, the switch S and diode of D_3 is turned off and the diodes of D_1, D_2 and D_4 are turned on. As a result, the inductors are discharged and the capacitors are charged.

3.1.1. Calculation of the capacitor voltage stress and boost factor

In this sub-section, the values of the boost factor and capacitor voltage stress in the one-cell HQZSI are calculated. By applying KVL into Fig. 2, we have:

$$v_{L1}=\begin{cases}-V_{C5}-V_{C3}-V_{C2} & ST\\ V_{C1} & nST\end{cases} \quad (1)$$

$$v_{L2}=\begin{cases}-V_{C5}-V_{C3}-V_{C1} & ST\\ V_{C2}=V_{C4} & nST\end{cases} \quad (2)$$

$$v_{L3}=\begin{cases}-V_{C5}-V_{C4}-V_{C1} & ST\\ V_{C3} & nST\end{cases} \quad (3)$$

$$v_{L4}=\begin{cases}V_{dc} & ST\\ V_{dc}+V_{C5} & nST\end{cases} \quad (4)$$

In above equations V_{dc}, v_{L1} to v_{L4} and V_{C1} to V_{C5} are the input dc voltage source, the voltage of the inductors L_1 to L_4 and the voltage of the capacitors C_1 to C_5, respectively.

According to the voltage balance in inductors and by considering the value of v_{L1} to v_{L4} from (1) to(4), the voltage of the capacitors are calculated as follows:

$$V_{C1}=V_{C2}=V_{C3}=V_{C4}=\frac{-D_{sh}}{(1-D_{sh})(1-3D_{sh})}V_{dc} \quad (5)$$

$$V_{C5}=\frac{-1}{1-D_{sh}}V_{dc} \quad (6)$$

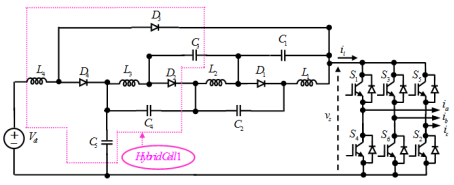


Fig. 2. The power circuit of the one-cell HQZSI topology with continuous current

By applying KVL into equivalent circuit of Fig. 2 in nST mode it is obtained that:

$$v_{s,\max}=-(V_{C5}+V_{C3}+V_{C2}+V_{C1})=\frac{1}{(1-3D_{sh})(1-D_{sh})}V_{dc} \quad (7)$$

In the HQZSI, the boost factor based on input voltage is calculated as follows:

$$B=\frac{v_{s,\max}}{V_{dc}}=\frac{1}{(1-3D_{sh})(1-D_{sh})} \quad (8)$$

As it is clear from (21), the value of boost factor in the proposed one-cell HQZSI is higher than the conventional ZSI which is equal to $B_{ZSI}=1/(1-D_{sh})$ with the same value of ST state duty cycle.

3.1.2. Diodes voltage stress calculation

By applying KVL in the equivalent circuit of Fig. 2, we have:

$$V_{D1}=\frac{-1}{(1-3D_{sh})(1-D_{sh})}V_{dc} \quad (9)$$

$$V_{D2}=\frac{-1}{(1-3D_{sh})(1-D_{sh})}V_{dc} \quad (10)$$

$$V_{D4}=\frac{-1}{1-D_{sh}}V_{dc} \quad (11)$$

By applying KVL in Fig. 2 in nST mode, the voltage stress of diode D_3 is equal to:

$$V_{D3}=V_{C1}+V_{C2}+V_{C3}=\frac{-3D_{Sh}}{(1-3D_{Sh})(1-D_{Sh})}V_{dc} \quad (12)$$

3.2. Proposed two-cell hybrid QZSI

By using two hybrid basic units, the two-cell HQZSI is proposed. The power circuit of this topology is shown in Fig. 3. As shown in this figure, the proposed topology includes of eight capacitors, seven diodes and six inductors. In ST state, the diodes of D_3 and D_5 are turned on and the diodes of D_1, D_2, D_4, D_6 and D_7 are turned off. As a result, the inductors are charged and the capacitors are discharged. In non-ST state, the diodes of D_3 and D_5 are turned off and the diodes of D_1, D_2, D_4, D_6 and D_7 are turned on. As a result, the inductors are discharged and the capacitors are charged.

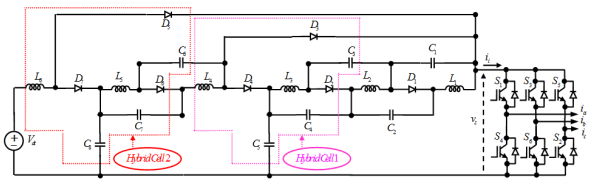


Fig. 3. The power circuit of the two-cell HQZSI topology with continuous current

3.2.1. Calculation of the Capacitor Voltage Stress and Boost factor

In this sub-section, the value of the boost factor and capacitor voltage stress in the proposed QZSI is calculated. By applying KVL in Figs. 3 and by considering this fact that the average voltage value of the inductor is equal to zero, we have:

$$V_{C1}=V_{C2}=V_{C3}=V_{C4}\frac{-D_{sh}}{(1-D_{sh})(1-2D_{sh})(1-3D_{sh})}V_{dc} \quad (13)$$

$$V_{C5}=\frac{-1}{(1-D_{sh})(1-2D_{sh})}V_{dc} \quad (14)$$

$$V_{C6}=V_{C7}=\frac{-D_{sh}}{(1-D_{sh})(1-2D_{sh})}V_{dc} \quad (15)$$

$$V_{C8}=\frac{-1}{1-D_{sh}}V_{dc} \quad (16)$$

$$v_{s,\max}=-(V_{C1}+V_{C2}+V_{C3}+V_{C5}) \quad (17)$$

Considering above equations, the value of boost factor is obtained as follows:

$$B=\frac{1}{(1-D_{sh})(1-2D_{sh})(1-3D_{sh})} \quad (18)$$

By comparing (8) and (18), it is obvious that by increasing the number of used hybrid basic unit, the value of boost factor is extremely increased

3.2.2. Diodes Voltage Stress Calculation

By applying KVL in the equivalent circuit of Fig. 3, we have:

$$V_{D1}=V_{D2}=\frac{-1}{(1-D_{sh})(1-2D_{sh})(1-3D_{sh})}V_{dc} \quad (19)$$

$$V_{D4}=V_{D6}=\frac{-1}{(1-D_{sh})(1-2D_{sh})}V_{dc} \quad (20)$$

$$V_{D7}=\frac{-1}{1-D_{sh}}V_{dc} \quad (21)$$

$$V_{D3}=\frac{-3D_{Sh}}{(1-D_{Sh})(1-2D_{Sh})(1-3D_{Sh})}V_{dc} \quad (22)$$

$$V_{D5}=\frac{6D_{sh}^2-5D_{sh}}{(1-D_{sh})(1-2D_{sh})(1-3D_{sh})}V_{dc} \quad (23)$$

3.3. Developed Proposed Hybrid QZSI

It is possible to increase the number of used Hybrid basic units to the conventional ZSI to generate developed HQZSI. The power circuit of this topology is shown in Fig. 4. As each hybrid basic unit consists of three capacitors, two inductances and three diodes, the numbers of used power electronic devices in the n-cell HQZSI are obtained as follows:

$$N_L=2n+2 \quad \& \quad N_C=3n+2 \quad \& \quad N_D=3n+1 \quad (24)$$

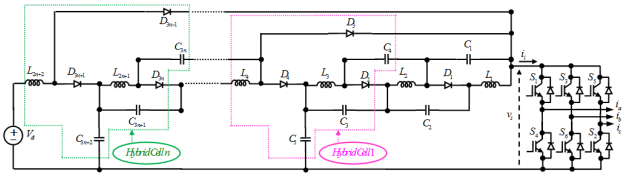


Fig. 4. The power circuit of the n-cell HQZSI topology with continuous current

3.3.1. Calculation of the Capacitor Voltage Stress and Boost factor

By comparing the voltage stress values of the capacitors C_1 to C_4 based on (5) and (13), it is clear that by increasing the number of used hybrid basic unit, these voltage values are same and are increased by the factor of $1/1-2D_{sh}$ in comparison to each other. As a result, the voltage stress values of the capacitors C_1 to C_4 in the n-cell HQZSI are obtained as follows:

$$V_{C1}=V_{C2}=V_{C3}=V_{C4}=\frac{-D_{sh}}{(1-D_{sh})(1-2D_{sh})^{n-1}(1-3D_{sh})}V_{dc} \quad (25)$$

Table 1. The capacitor voltage stress values and boost factors in HQZSI based on different number of used basic units

	Number of used hybrid basic units			
	1	2	3	4
V_{C5}/V_{dc}	$-K_1$	$-K_1K_2$	$-K_1K_2^2$	$-K_1K_2^3$
V_{C6}/V_{dc}	-	$-D_{sh}K_1K_2$	$-D_{sh}K_1K_2^2$	$-D_{sh}K_1K_2^3$
V_{C7}/V_{dc}	-	$-D_{sh}K_1K_2$	$-D_{sh}K_1K_2^2$	$-D_{sh}K_1K_2^3$
V_{C8}/V_{dc}	-	$-K_1$	$-K_1K_2$	$-K_1K_2^2$
V_{C9}/V_{dc}	-	-	$-D_{sh}K_1K_2$	$-D_{sh}K_1K_2^2$
V_{C10}/V_{dc}	-	-	$-D_{sh}K_1K_2$	$-D_{sh}K_1K_2^2$
V_{C11}/V_{dc}	-	-	$-K_1$	$-K_1K_2$
V_{C12}/V_{dc}	-	-	-	$-D_{sh}K_1K_2$
V_{C13}/V_{dc}	-	-	-	$-D_{sh}K_1K_2$
V_{C14}/V_{dc}	-	-	-	$-K_1$
B	K_1K_3	$K_1K_2K_3$	$K_1K_2^2K_3$	$K_1K_2^3K_3$
Description	$K_1=\frac{1}{(1-D_{sh})}$, $K_2=\frac{1}{(1-2D_{sh})}$, $K_3=\frac{1}{(1-3D_{sh})}$			

The voltage stress values of other capacitors and the value of the boost factor in the proposed HQZSI based on using different number of hybrid basic units are summarized in Table 1. According to this Table, by adding each hybrid basic unit, three capacitors are added in a way that the capacitor voltage stress for two of them are same and are equal to the capacitor voltage stress in the previous topology. The voltage stress values of the other capacitors C_5 to C_{3n+2} in the n-cell HQZSI are obtained as follows:

$$V_{C3n+2}=-V_{dc}/(1-D_{sh}) \quad (26)$$

$$V_{C3m+1} = V_{C3m} = \frac{D_{sh}}{(1-2D_{sh})} V_{C3m+2} \quad for\ m = 2,3,\ldots,n \tag{27}$$

$$V_{C3m-1} = \frac{1}{(1-2D_{sh})} V_{C3m+2} \quad for\ m = 2,3,\ldots,n \tag{28}$$

In addition, the maximum inverter input voltage value is equal to:

$$v_{s,\max} = -(V_{C1} + V_{C2} + V_{C3} + V_{C5}) \tag{29}$$

Under this the value of boost factor is obtained as follows:

$$B = \frac{1}{(1-D_{sh})(1-2D_{sh})^{n-1}(1-3D_{sh})} \tag{30}$$

By comparing the equations of (8), (18) and (30), it is clear that by increasing the number of hybrid basic unit, the value of boost factor is extremely increased by the factor of $1/1-2D_{sh}$ without using any additional active elements.

3.3.2. Diodes Voltage Stress Calculation

The diodes voltage stress values in the proposed HQZSI based on using different hybrid basic units are summarized in Table 2.

Table 2. The diodes voltage stress values in HQZSI based on different number of used basic units

	Number of used hybrid basic units			
	1	2	3	4
V_{D1}/V_{dc}	$-K_1K_3$	$-K_1K_2K_3$	$-K_1K_2^2K_3$	$-K_1K_2^3K_3$
V_{D2}/V_{dc}	$-K_1K_3$	$-K_1K_2K_3$	$-K_1K_2^2K_3$	$-K_1K_2^3K_3$
V_{D3}/V_{dc}	$-3D_{sh}K_1K_3$	$-3D_{sh}K_1K_2K_3$	$-3D_{sh}K_1K_2^2K_3$	$-3D_{sh}K_1K_2^3K_3$
V_{D4}/V_{dc}	$-K_1$	$-K_1K_2$	$-K_1K_2^2$	$-K_1K_2^3$
V_{D5}/V_{dc}	-	$K_1K_2K_3K_4$	$K_1K_2^2K_3K_4$	$K_1K_2^3K_3K_4$
V_{D6}/V_{dc}	-	$-K_1K_2$	$-K_1K_2^2$	$-K_1K_2^3$
V_{D7}/V_{dc}	-	$-K_1$	$-K_1K_2$	$-K_1K_2^2$
V_{D9}/V_{dc}	-	-	$-K_1K_2$	$-K_1K_2^2$
V_{D10}/V_{dc}	-	-	$-K_1K_2$	$-K_1K_2^2$
V_{D12}/V_{dc}	-	-	-	$-K_1K_2$
V_{D13}/V_{dc}	-	-	-	$-K_1$
Description	$K_1 = 1/(1-D_{sh})$, $K_2 = 1/(1-2D_{sh})$, $K_3 = 1/(1-3D_{sh})$, $K_4 = 6D_{sh}^2 - 5D_{sh}$			

According to this Table, the voltage values of diodes D_1 and D_2 are equal to each other. In addition, by increasing the number of used hybrid basic units, three diodes are added that one of them is connected parallel to the topology and the other is series connected to the previous topology. In this condition, the voltage of the last connected diode in the new topology is equal to the voltage value of last diode in previous structure. The voltage stress values of diodes in the n-cell HQZSI are obtained as follows:

$$V_{D1} = V_{D2} = \frac{-1}{(1-D_{sh})(1-2D_{sh})^{n-1}(1-3D_{sh})} V_{dc} \tag{31}$$

$$V_{D3} = \frac{-3D_{Sh}}{(1-D_{Sh})(1-2D_{Sh})^{n-1}(1-3D_{Sh})} V_{dc} \tag{32}$$

$$V_{D5} = \frac{6D_{sh}^2 - 5D_{sh}}{(1-D_{sh})(1-2D_{sh})^{n-1}(1-3D_{sh})} V_{dc} \tag{33}$$

$$V_{D3n+1} = -V_{dc}/(1-D_{sh}) \tag{34}$$

$$V_{D3m-2} = V_{D3m} = \frac{1}{(1-2D_{sh})} V_{D3m+1} \quad for\ m = 2,3,\ldots,n \tag{35}$$

4. Simulation results

In this section, in order to reconfirm the correct performance of the proposed topology the simulation results on the two-cell HQZSI in EMTDC/PSCAD software are used. The topology that is shown in Fig. 2 is used in this simulation. The values of different elements are summarized in Table 3. In addition, all elements are considered ideally and the simple boost control method is used.

Table 3. The used parameters in simulation

V_i	$50V$	$L_{1\ to\ 6}$	6 mH
f_s	$5kHz$	$C_{1\ to\ 8}$	680 μF
R_L	150Ω	D_{ST}	0.15
L_f	55 mH	f_o	50Hz

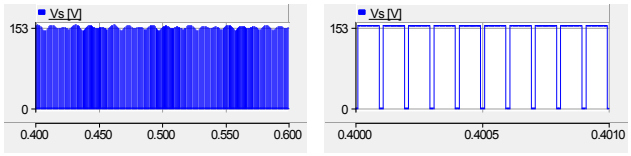
Fig. 5 shows the input voltage waveform to the inverter. As shown in Fig. 5(a), the maximum input voltage value to the inverter is equal to $153V$ that is close to its obtained value from (17) which is $152.76V$. In addition, the extended input voltage value is shown in Fig. 5(b). According to this figure, the value of boost factor from simulation result is near to 3 while the obtained boost factor from (18) is equal to 3.05.

The output voltage waveforms of used capacitors are shown in Fig. 6. As shown in Fig. 6(a), the voltage values of the capacitors C_1 to C_4 are same as to each other and equal to $23V$. This value verifies the obtained capacitor voltage value based on (13) that is equal to $22.91V$. The voltage waveform of the capacitor C_5 is shown in Fig. 6(b). According to this figure, the capacitor voltage value is equal to $85V$ that is close to its obtained value from (14) which is $84.03V$. Fig. 6(c) indicates the voltage value of the capacitor C_6 and C_7 which are equal to $13V$. This value is close to its obtained value from (15) that is $12.6V$. Fig. 6(d) shows the voltage value of the capacitor C_8 which is equal to $59V$. This value is close to its obtained value from (16) that is $58.8V$.

Fig. 7(a) shows the voltage of diodes D_1, D_2 and their extended waveforms. The voltage waveforms of other diodes are shown in Figs. 7(b) to 7(e). According to these figures the diodes voltage values are equal to $153V$, $72V$, $85V$, $96V$ and $59V$, respectively. These values are close to the obtained values theoretically.

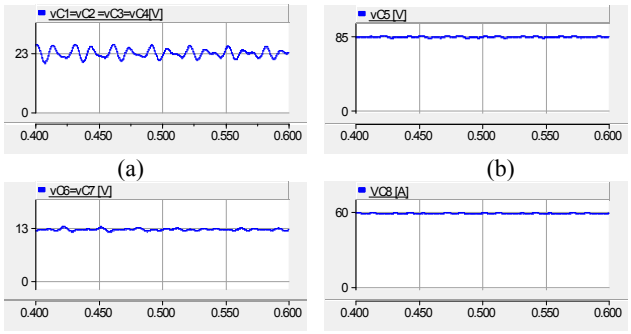
The output voltage and current waveforms of the proposed HQZSI are shown in Fig. 8. As shown in this figure, the proposed inverter is able to generate sinusoidal waveform with

the maximum amplitude of 135 at the output. In addition, there is a phase shift between voltage and current waveforms.



(a) (b)

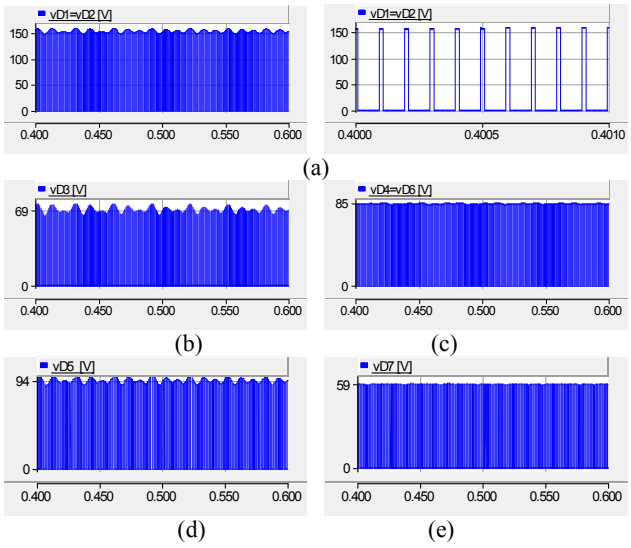
Fig. 5. (a) The input voltage waveforms to the inverter of the proposed two-cell HQZSI; (b) Extended input voltage to the inverter



(a) (b)

(a) (b)

Fig. 6. Capacitors voltage waveforms; (a) $V_{C1}=V_{C2}=V_{C3}=V_{C4}$; (b) V_{C5}; (c) $V_{C6}=V_{C7}$; (d) V_{C8}



(a)

(b) (c)

(d) (e)

Fig. 7. Diodes voltage waveforms; (a) $V_{D1}=V_{D2}$; (b) V_{D3}; (c) $V_{D4}=V_{D6}$; (d) V_{D5}; (e) V_{D7}

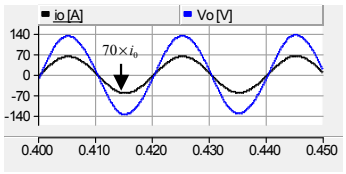


Fig. 8. The output voltage and current waveform

5. CONCLUSION

In this paper, a new developed topology for quasi Z-source inverter is proposed. This topology is based on new hybrid basic unit that is combination of diode and capacitor cells. The proposed inverter is completely analyzed and the related equations of diode voltage stress, capacitor voltage stress and boost factor are obtained. According to these equations, the value of boost factor in the n-cell HQZSI is obtained by the equation of $B=1/(1-D_{sh})(1-2D_{sh})^{n-1}(1-3D_{sh})$. This means that it is possible to obtain the desire value of boost factor without using any additional active element. In addition, the value of boost factor in this topology is increased by the factor of $1/1-D_{sh}$ in comparison to the conventional ZSI while the same value of duty cycle is used. The common earth connection is the other advantages of the proposed inverter. Finally, the correct performance of the proposed HQZSI is verified through simulation results.

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