Effect of LED Wiring and Cabling Topologies on Visible Light Communication Channels

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Abstract

Visible light communication (VLC) is an emerging short-range wireless access technology. It involves the dual use of illumination infrastructure for communication purposes and builds upon the principle of modulating light emitting diodes (LEDs) at very high speeds that are not noticeable to the human eye. Although there has been a growing literature on VLC channel modeling, the existing works mainly overlook the effects of wiring and cabling topologies. Wiring topology refers to how LED chips are connected within the luminaire while cabling topology refers to how the luminaires are connected to the communication access point. In this paper, we adopt ray-tracing based VLC channel modeling approach and consider various cabling/wiring topologies. For each topology, we obtain channel impulse responses (CIRs) and quantify the impact of wiring and cabling delays.

1. Introduction

Visible light communication (VLC) is an emerging short-range wireless access technology [1]. It involves the dual use of illumination infrastructure for communication purposes and builds upon the principle of modulating light emitting diodes (LEDs) at very high speeds that are not noticeable to the human eye [2]. With powerful features such as operation in unlicensed optical spectrum, high bandwidth and immunity to electromagnetic interference, VLC is considered as a powerful alternative to radio-frequency (RF) wireless solutions.

Although there has been a growing literature on VLC systems, see e.g., [3] for an extensive survey, the existing works mainly overlook the characteristics of lighting infrastructure and luminaire design that might have implications for VLC system design. A luminaire typically consists of multiple LED chips. Wiring topology refers to how LED chips are connected within the luminaire. In a typical indoor environment, there exist multiple luminaires. Cabling topology refers to how the luminaires are connected to the communication access point. Based on the type and lenght of cabling/wiring, significant delays can be introduced which should be taken into account in channel modeling.

Recently, there has been an extensive work on VLC channel modeling including both fixed [4-9] and mobile [10-12] scenarios. These works discuss several indoor scenarios and lighting conditions. However, to the best of our knowledge, there is only one previous work that discusses the effect of cabling and wiring topologies [13]. In [13], Ren *et al.* introduce a recursive channel model based on Barry's method [9] taking into account wiring and cabling delays. The work in [13] is limited to the assumptions of only purely diffuse reflections and ideal Lambertian source which might not hold true for many practical cases. In this paper, we adopt ray-tracing based VLC channel modeling approach [8] and consider various cabling/wiring topologies. For each topology, we obtain channel impulse responses (CIRs) and quantify the impact of wiring and cabling delays on CIRs.

The remainder of the paper is organized as follows. In Section 2, we describe the adopted channel modeling approach. In Section 3, we present a number of cabling and wiring topologies to be investigated. In Section 4, we present CIRs for the topologies under consideration and discuss the effect of cabling and wiring delays on channel frequency selectivity. Finally, we conclude in Section 5.

2. VLC Channel Modeling

In this work, we assume the deployment of multiple ceiling luminaires where each LED luminaire consists of multi LED chips. Assume that there are N_L luminaires and each luminaire includes N_C LED chips.

Let $h_i(t),\ i = 1, ..., N_C$ denote the individual optical CIR between the i^{th} LED chip and the receiver. It can be expressed as

$$h_i(t) = \sum_{j=1}^{N_r} P_{i,j}\ \delta(t - \tau_{i,j}) \tag{1}$$

where $P_{i,j}$ is the optical power of the j^{th} ray from the i^{th} LED chip, $\tau_{i,j}$ is the propagation time of the j^{th} ray from the i^{th} LED chip, $\delta(t)$ is the Dirac delta function and N_r is the number of rays received at the detector.

The optical CIR between the k^{th} luminaire $k = 1, ..., N_L$ and the receiver can be expressed as

$$h_k(t) = \sum_{i=1}^{N_C} h_i(t - \tau_{W_i}) \tag{2}$$

where τ_{W_i} is the wiring delay of the i^{th} LED chip and N_C is the number of LED chips inside the k^{th} luminaire. The overall optical CIR is then given as

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$$h(t) = \sum_{k=1}^{N_L} h_k(t - \tau_{C_k}) = \sum_{k=1}^{N_L} \sum_{i=1}^{N_C} \sum_{j=1}^{N_r} P_{i,j}\ \delta(t - \tau_{i,j} - \tau_{W_i} - \tau_{C_k}) \quad (3)$$

where τ_{C_k} is the cabling delay of the k^{th} luminaire and N_L is the number of ceiling luminaires.

For channel modelling, we use the ray tracing approach described in [8]. The simulation environment is created in Zemax® and enables us to specify the geometry of the environment, the objects within as well as the specifications of the sources (i.e., LEDs) and receivers (i.e., photodiodes). For a given number of rays and the number of reflections, the non-sequential ray tracing tool calculates the detected power and path lengths from source to detector for each ray. These are then imported to Matlab® and processed to yield the CIR formulated in (3).

The frequency response of the optical channel can be further obtained through the Fourier transform, i.e.,

$$H(f) = F[h(t)] = \int_{-\infty}^{\infty} \sum_{k=1}^{N_L} \sum_{i=1}^{N_C} \sum_{j=1}^{N_r} P_{i,j}\ \delta(t - \tau_{i,j} - \tau_{W_i} - \tau_{C_k}) e^{-j2\pi t} dt \quad (4)$$

3. Cabling and Wiring Topologies

In a typical indoor environment, there exist multiple luminaires. The LED luminaires are designed to operate with available AC electric sources. Since the available AC sources have fixed voltages, e.g., 120V, 220V or 240V, the LED luminaires are connected in parallel to have the same voltage over all luminaires. We assume that a data cable (CAT 5) runs in parallel to the electrical cable. It is also possible to use power over ethernet (PoE) to feed both data and power. In Fig. 1, we consider the layout of four LED ceiling luminaires denoted as $L_k,\ k = 1, ..., 4$. Each luminaire includes 4 LED chips denoted as $C_{k,i},\ i = 1, ..., 4$, and $k = 1, ..., 4$. We assume the deployment of a central access point (AP) where the LED luminaires (that act as transmitters) are connected. For connection, we consider two cabling topologies. In the first topology (Fig. 1.a), the data/electrical cables are terminated at the middle of luminaires. The length of cable between the access point and each luminaire is the same. In the second topology (Fig. 1.b), cables feed the luminaire from the side. The lenght of cable for each luminaire changes in this case. Difference in two topologies will not have any affect on illumination performance but the communication performance might be affected due to different cable lengths. For instance, when a signal is sent from AP to luminaires, all of the luminaires in Fig. 1.a would receive it at the same time. On the other hand, in Fig. 1.b, luminaire pairs (L_2 and L_3) and (L_1 and L_4) would receive it at the same time. But there would be a particular delay between two pairs based on the cable length differences.

The wiring topology is more complicated than the cabling topology. In an LED luminaire, the LED chips can be connected in series, in parallel or some combination. The choice of wiring topology mainly depends on the type and characteristics of LED chips, their driving forward current (I_f) and forward voltage (V_f) as well as the output current and voltage of the power supply unit (PSU) in the LED luminaire. There are two types of PSU, i.e., constant current PSU and constant voltage PSU. A constant current PSU has an output of fixed current

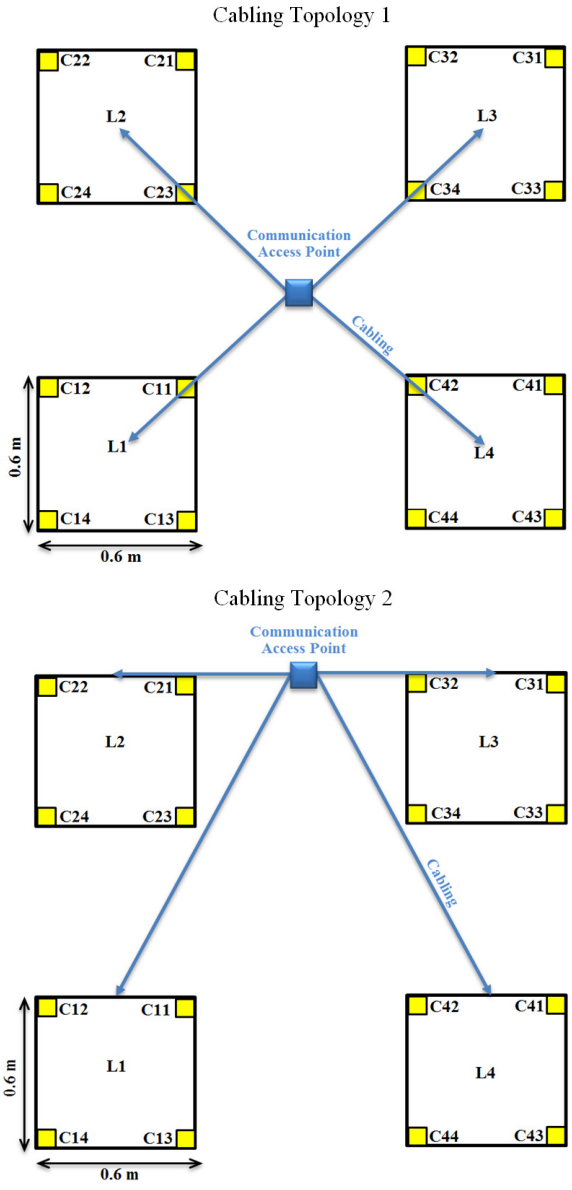

Fig. 1. Cabling topologies under consideration

with a variable voltage within a particular range. These PSUs vary the voltage with respect to load to keep the current constant. On the other hand, a constant voltage PSU does the reverse, i.e., varies the current within a range to keep the output voltage constant. In LEDs, because of the significant changes in I_f and relative luminous flux with small changes in V_f, constant current PSUs are typically preferred to have more control over total light output of luminaires and uniformity of light output of LEDs of a luminaire. To ensure the same or similar light outputs for uniformity purposes, all of the LED chips are typically driven at the same forward current.

According to the above considerations, four different wiring topologies are presented in Fig. 2. Without loss of generalization, only the luminaire L_1 is considered. In Figs. 2.a and 2.b, four LED chips $C_{1,i},\ i = 1, ..., 4$ are connected in series. In Figs. 2.c and 2.d, LED chips are connected in parallel. In Figs. 2.a and 2.b, all of the four LED chips would have the same I_f as desired for uniform illumination. In Figs. 2.c and

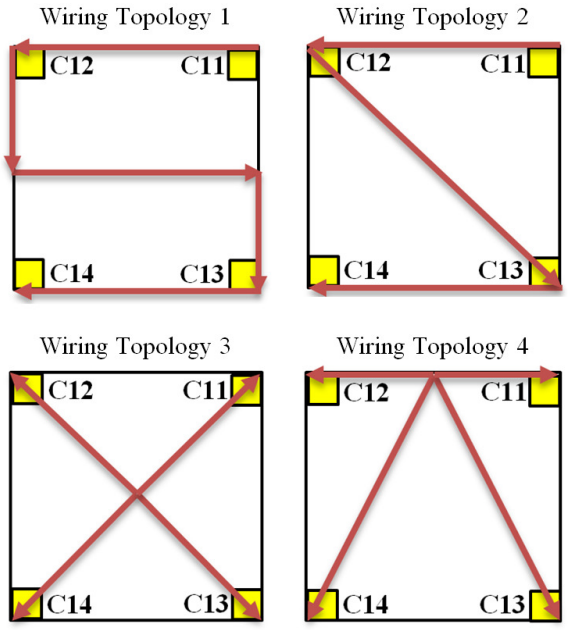

Fig. 2. Wiring topologies under consideration

2.d, all of the four LED chips would have the same V_f values. This indicates that similar I_f values will flow through each LED chip if their V_f differences are sufficiently low.

4. Simulation Results and Discussions

In the simulation study, we consider a room with dimensions of 5 m × 5 m × 3 m as illustrated in Fig. 3. Considering the layout in Fig. 1, we assume four luminaires as $L_k,\ k = 1, ..., 4$ on the ceiling with equidistance spacing of 2 m. The LED luminaire has a square shape with size of 0.6 m × 0.6 m and consists of 4 LED chips as $C_{k,i},\ i = 1, ..., 4$. Each LED chip radiates 5 W with a view angle of 120°. Four photodetectors (PDs) denoted as $D_l,\ l = 1, ..., 4$ are placed on the table at a height of 0.8 m. The FOV semi-angle and area of the PD are 85° and 1 cm^2, respectively. The cabling and wiring delay values are $\tau_{C_k} = 5$ ns/m [14] and $\tau_{W_i} = 6.5$ ns/m [15], respectively. The simulation parameters are summarized in Table I.

First, we consider cabling topologies 1 and 2 and ignore the wiring delays[1]. As a benchmark, we further consider the hypothetical case where the cables are delay-free. Based on (3), the overall optical CIR $h(t)$ as seen by the photodetector D_1 is presented in Fig. 4. It is observed from Fig. 4 that in topology 1, we have one large peak and then one small. Since the cabling delays of four luminaires are the same, the signals from each luminaire are received at the same time. This results in one large peak followed by a small peak, the latter results from multipath reflections. In topology 2, it is observed that we have two large peaks followed by a small one. Two large peaks come from luminaire pairs (L_2 and L_3) and (L_1 and L_4). It can be also noted that for the hypothetical case where the cables are delay-free, we have one large peak followed by a small one similar to topology 1. However, the large peak in this case occurs at 9 ns while the large peak in topology 1 occurs at 16 ns which is the result of cabling delay.

[1]We ignore the effect of path loss related to data cables. In practice, an amplifier is used at VLC-enabled LED luminaire. Such an amplifier can be used to mitigate the effect of such losses.

Table 1. Simulation parameters for scenario under consideration

Parameters	Values
Room Parameters	
Size of Room (L × W × H)	5 m × 5 m × 3 m
Room	Wall: Plaster Floor: Pinewood Ceiling: Plaster
Furniture	Desk: Pinewood
Transmitter Parameters	
Size of luminaire	0.6 m × 0.6 m
Number of luminaire	4
Distance between luminaires	2 m
Number of LED chip per each luminaire	4
Power of each LED chip	5 W
View angle of LED chip	120°
Cabling delay (τ_{C_k})	5 ns/m
Wiring delay (τ_{W_i})	6.5 ns/m
Receiver Parameters	
Number of PD	4
FOV of PD	85°
Area of PD	1 cm^2
Distance between PD	0.1 m

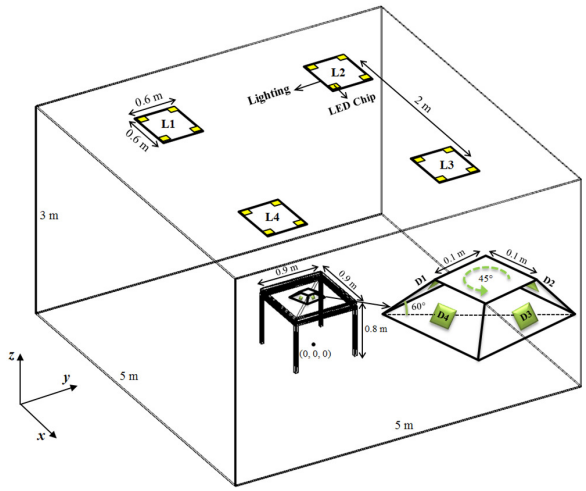

Fig. 3. Scenario under consideration

Second, we consider wiring topologies 1, 2, 3 and 4 and ignore the cabling delays. As a benchmark, we further consider the hypothetical case where the wires are delay-free. Based on (2), the optical CIR $h_1(t)$ between luminaire L_1 and photodetector D_1 is presented in Fig. 5. It is observed from Fig. 5 that in wiring topologies 1 and 2, we have four large peaks followed by a small one. Four large peaks comes from LED chips $C_{1,1}$, $C_{1,2}$, $C_{1,3}$ and $C_{1,4}$ while the small one results from multipath reflections. In topology 3, it is observed that we have one large peak and then one small. This is as a result of the fact that the wiring delays of four LED chips are the same. In topology 4, it is observed that we have two large peaks and then one small. Two large peaks comes from LED chip pairs ($C_{1,1}$ and $C_{1,2}$) and ($C_{1,3}$ and $C_{1,4}$). For the hypothetical delay-free case, we have one large peak and then one small similar to topology 3. It should be of course noted that the large peak in this case occurs at 9 ns, however, the large peak in topology 3 occurs at 13 ns which is the result of wiring delay.

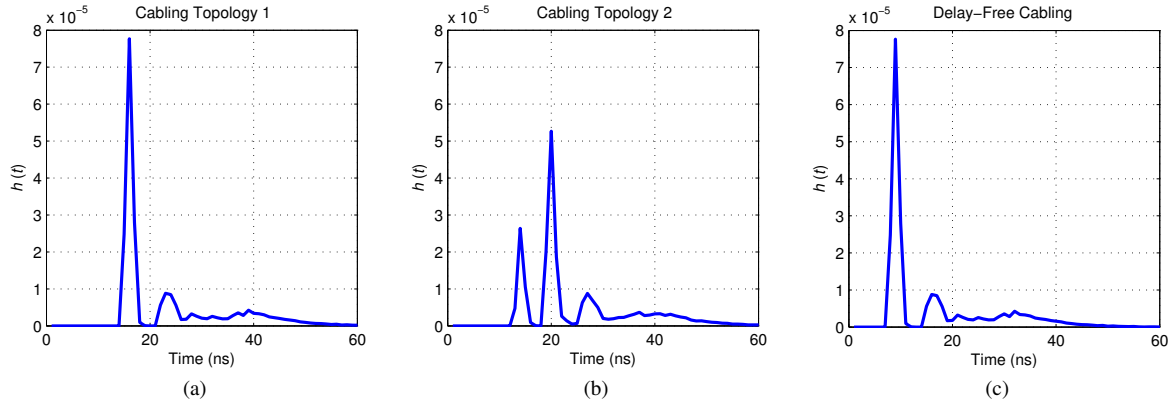

Fig. 4. Overall optical CIRs (as received by the photodetector D_1) for (a) cabling topology 1, (b) cabling topology 2 and (c) delay-free cabling

Finally, we consider the effects of both wiring and cabling topologies in Fig. 6. We assume the use of cabling topology 1 in conjunction with wiring topology 1 and 3. The hypotethical case of delay-free wiring and cabling is further included as a benchmark. It is observed from Fig. 6.a. that for cabling topology 1 in conjunction with wiring topology 1, we have four large peaks followed by a small one. The CIR is similar to what is obtained for wiring topology presented in Fig. 5a. This indicates that the wiring topology is dominant for the channel characterization. Since the CIR shown in Fig. 6.a is composed of the CIRs from four luminaires, its amplitude is larger than that one shown in Fig. 5.a. Additionally, the first peak in the CIR presented in Fig. 5.a (where wiring topology 1 is considered and cabling delay is ignored) occurs at 8 ns while the first peak of CIR in Fig. 6.a (where the combined effect of cabling topology 1 and wiring topology 1 is considered) occurs at 15 ns as a result of cabling delay. It is further observed from the comparison of Fig. 6.b and Fig. 6.c that the CIR for the case of cabling topology 1 and wiring topology 3 has a similar behaviour to the ideal case with only some delay. This is a result of the fact that cabling topology 1 and wiring topology 3 have symmetrical structures. In other word, all luminaires in cabling topology 1 and all LED chips in wiring topology 3 have identical cabling and wiring delays, respectively. Such a symmetrical wiring/cabling structure results in only an overall shift of the CIR.

The corresponding channel frequency responses of overall CIRs for these three cases are further illustrated in Fig. 7. It is observed that frequency selectivity is introduced with respect to the ideal case of delay-free wiring and cabling. This will introduce limitations on the transmission bandwidth. According to the well known 3dB-bandwidth definition [16], the bandwidth for the ideal case can be calculated as 12.74 Mb/s. This remains the same for the case where cabling topology 1 and wiring topology 3 are considered due to symmetrical structure. This reduces to 9.70 Mb/s for cabling topology 1 and wiring topology 1 where frequency selectivity is more pronounced.

5. Conclusions

In this paper, we have investigated the effect of data cables that run between the communication access point and LEDs as well as wiring topologies within the LED luminaire on the VLC channel. We have considered a number of cabling/wiring topologies and obtained CIRs for each. It is observed that cabling and wiring introduce delays that might significantly affect the overall channel characteristics. Our results reveal that the effect of wiring topology is pronounced more with respect to cabling topology and wiring topology becomes the determining factor. Furthermore, it is observed that symmetrical cabling and wiring topologies are more favorable from communication system design perspective.

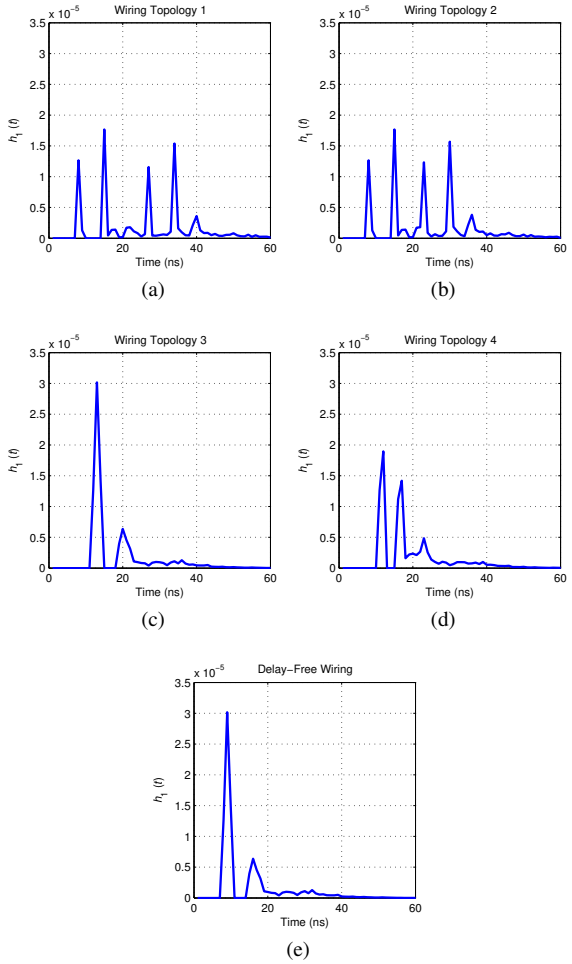

Fig. 5. Optical CIRs from the luminaire L_1 (as received by the photodetector D_1) for (a) wiring topology 1, (b) wiring topology 2, (c) wiring topology 3, (d) wiring topology 4 and (e) delay-free wiring

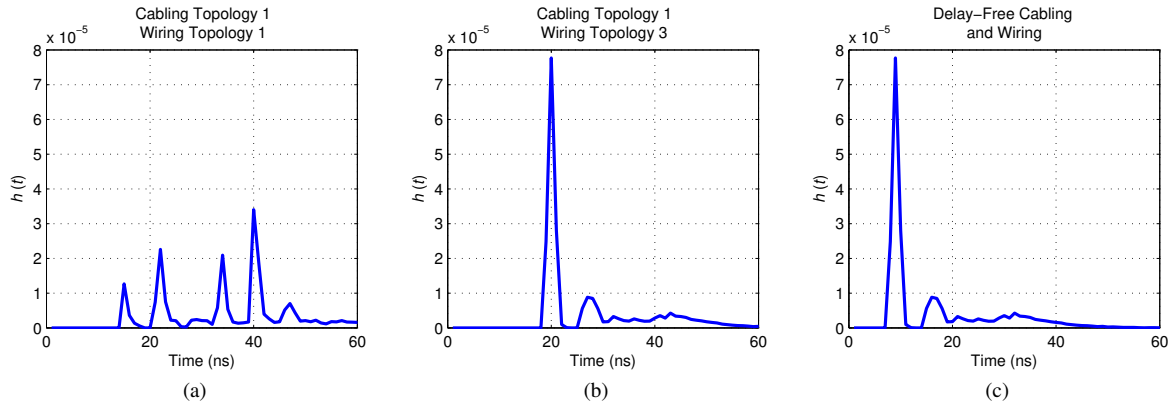

Fig. 6. Overall optical CIRs (as received by the photodetector D_1) for (a) cabling topology 1 and wiring topology 1, (b) cabling topology 1 and wiring topology 3 and (c) delay-free cabling and wiring

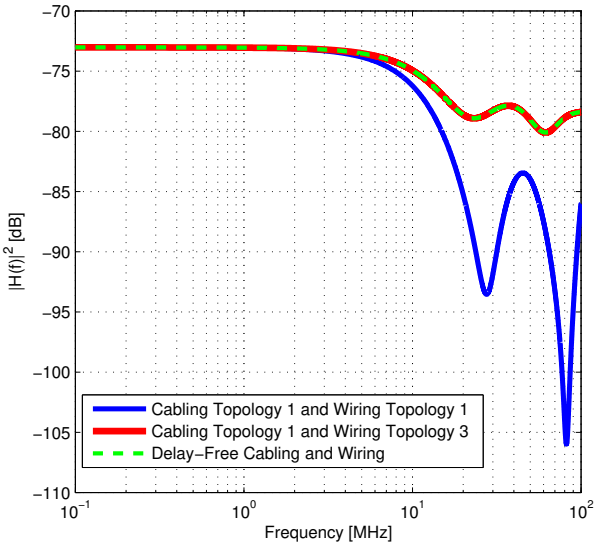

Fig. 7. Channel frequency response of overall optical CIRs considering the combined effect of cabling and wiring delays

6. References

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