Single Active Device MetaMutator; its Application to Impedance Simulation and in particular to FDNR

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Abstract

The proposed Metamutator configuration employs only one Fully Differential Current Conveyor (FDCCII) which has 9 terminals including ground. By properly interconnecting these terminals a 4-port Metamutator is obtained without use of any other external element. It maintains the following advantages: (i) use of only one active element: less is the number of active devices less is the amount of disparity, (ii) possibility of realizing Memristors, Capacitors, Inductors, Frequency Dependent Negative Resistor (FDNR), which can be used to make integrated circuit active filters, (iii) no need to impose component choice constraints. SPICE simulations' results using TSMC 0.18µm CMOS process parameters and ±0.9V supply voltages validate the theoretical predictions.

1. Introduction

The first hard-realization of Memristor introduced in [1], was achieved in the same paper using Mutators. Since then many types of mutator circuits have been proposed for realizing memristors with nonlinear resistors and also meminductors or memcapacitors [1-7]. Newly a new multipurpose 4-port, which has been introduced in [8] and named Metamutator in [9], has been shown capable to implement a variety of elements/systems like memstors*, quadrature oscillators, amplifiers and voltage mode universal filters when some of the ports are properly terminated. Several IC designs of Metamutators have been proposed and discussed in [8-10].

Recently, Impedance simulators, gyrators, FDNR simulators are being produced by several manufacturers and many realizations have been given [11-14]. In the structure of many of these circuits two or more active devices are employed. For example in [14] a FDNR simulator with three DO-CCIIs, three resistors and one capacitor are used; furthermore the proposed circuits require component matching. Analog Devices, in the data sheet of BiFET OpAmp AD711 exhibits a 9-pole Chebyshev filter using four FDNRs and 2 OpAmps [15]. As it is well known the difference between ideal and simulated responses mainly occurs from the parasitic elements and non-ideal gain effects of the active devices so the less number of active devices causes less amount of disparity. The novel proposed circuit has an advantage over earlier circuits because of the number of active and passive components, a simpler circuitry consisting of only one active device and three passive components and, as a result no need of matching components and functionality.

The newly inspired Metamutator circuit with its port description and its use for realizing a memristor will be given in Section II. The theoretical derivation of Capacitance Multiplier, Inductor Simulator and FDNR will be given in Section III. The PSpice simulation results of all these devices using the new Metamutator realized with TSMC 0.18 µm process parameters, ±0.9 V and 0.24 V supply voltages are shown in Section IV. Finally, Section V concludes the paper.

2. Newly Proposed Metamutator

The block diagram of a 4-port Voltage Inverting Metamutator (VIM) and its port description matrix are given in Fig. 1 and (1).

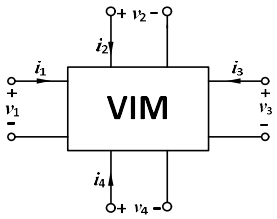

Fig. 1. Block diagram of VIM 4-port metamutator [11]

$$\begin{bmatrix} i_1 \\ i_3 \\ v_2 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} i_2 \\ i_4 \\ v_3 \\ v_1 \end{bmatrix} \quad (1)$$

The block diagram of the Fully Differential Current Conveyor (FDCCII), used in building newly proposed Metamutator circuit, is shown in Fig. 2 and its port description matrix in (2),

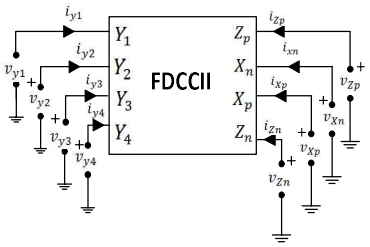

Fig. 2. Block diagram of FDCCII

$$\begin{bmatrix} v_{xp} \\ v_{xn} \\ i_{zp} \\ i_{zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{xp} \\ i_{xn} \\ v_{y1} \\ v_{y2} \\ v_{y3} \\ v_{y4} \end{bmatrix} \quad (2)$$

$$i_{y1} = i_{y2} = i_{y3} = i_{y4} = 0$$

With proper interconnections of port branches as shown in Fig. 3, one can convert the FDCCII to a Metamutator thus realized with a single active device (terminals Z_p and Z_n are grounded.)

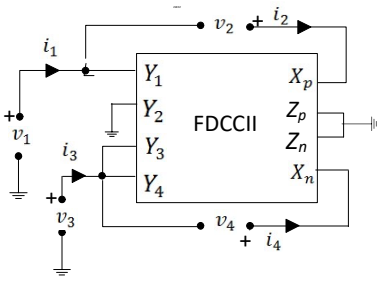

Fig. 3. Block diagram of metamutator with FDCCII

As the ports description matrix of this newly proposed metamutator is the same as (1), the Table 2 [8] stands true for this metamutator.

For example according to Table 2 in [8], by connecting an inductor to port 4, a nonlinear resistor to port 3 and a capacitor to port 2 of the metamutator with FDCCII, using KVL and KCL a memristor will be observed from port 1. For this case the circuit structure is illustrated in Fig. 6.

The following chain of equalities using port description matrix of metamutator and Kirchoff's Laws yield:

$$f(-i_3, v_3) = 0 \tag{3}$$

Replacing i_3, v_3 with i_4, v_2 respectively using (1), gives:

$$f(-i_4, v_2) = 0 \tag{4}$$

Element defining relations $i_4 = \frac{\varphi_4}{L}$ and $v_2 = \frac{q_2}{C}$ used in (4) gives:

$$f\left(-\frac{\varphi_4}{L}, \frac{q_2}{C}\right) = 0 \tag{5}$$

Finally, use of (1) again to replace φ_4 and q_2 by $-\varphi_1$ and q_2 respectively, yields the memristor's scaled constitutive relation shown in (6), at port 1.

$$f\left(\frac{\varphi_1}{L}, \frac{q_1}{C}\right) = 0 \tag{6}$$

The simulation results will be given in the next sections.

3. Application of Metamutator as Impedance Multiplier and Simulator

The general structure of Metamutator with port ımpedances is shown in Fig.4 and Z_1can be calculated as $Z_1 = Z_2Z_4/Z_3$.

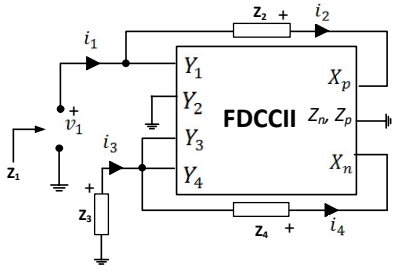

Fig. 4. Metamutator terminated with port impedances.

Similarly the impedance seen from another port by connecting impedances to the other three ports is depicted in Table 1. A nice conclusion that can be deduced from Table 1 is that this new configuration of the Metamutator allows the realization of grounded elements as well as floating ones.

Table 1. Impedance of the ports

Ports	Port 1	Port 2	Port 3	Port 4
Type	Grounded	Floating	Grounded	Floating
Impedance	$Z_1 = \frac{Z_4}{Z_3}.Z_2$	$Z_2 = \frac{Z_3}{Z_4}.Z_1$	$Z_3 = \frac{Z_2}{Z_1}.Z_4$	$Z_4 = \frac{Z_1}{Z_2}.Z_3$

3.1. Application as Capacitance Multiplier

According to Table1 replacing one capacitor and two resistors in three of the ports properly a capacitor will be achieved at the fourth port in which the amount of capacitance is equal to the amount of the capacitor multiplied by the ratio of resistance values. The different realizations are shown in Table 2.

Table 2. Different realizations of capacitance multiplier

Realization	Port 1	Port 2	Port 3	Port 4	Capacitance
#1	C_{eq}	C_2	R_3	R_4	$\frac{1}{sC_{eq}} = \frac{R_4}{sC_2R_3} \rightarrow C_{eq} = C_2.\frac{R_3}{R_4}$
#2	C_{eq}	R_2	R_3	C_4	$\frac{1}{sC_{eq}} = \frac{R_2}{sC_4R_3} \rightarrow C_{eq} = C_4.\frac{R_3}{R_2}$
#3	R_1	C_{eq}	C_3	R_4	$\frac{1}{sC_{eq}} = \frac{R_1}{sC_3R_4} \rightarrow C_{eq} = C_3.\frac{R_4}{R_1}$
#4	C_1	C_{eq}	R_3	R_4	$\frac{1}{sC_{eq}} = \frac{R_3}{sC_1R_4} \rightarrow C_{eq} = C_1.\frac{R_4}{R_3}$
#5	R_1	C_2	C_{eq}	R_4	$\frac{1}{sC_{eq}} = \frac{R_4}{sC_2R_1} \rightarrow C_{eq} = C_2.\frac{R_1}{R_4}$
#6	R_1	R_2	C_{eq}	C_4	$\frac{1}{sC_{eq}} = \frac{R_2}{sC_4R_1} \rightarrow C_{eq} = C_4.\frac{R_1}{R_2}$
#7	C_1	R_2	R_3	C_{eq}	$\frac{1}{sC_{eq}} = \frac{R_3}{sC_1R_2} \rightarrow C_{eq} = C_1.\frac{R_2}{R_3}$
#8	R_1	R_2	C_3	C_{eq}	$\frac{1}{sC_{eq}} = \frac{R_1}{sC_3R_2} \rightarrow C_{eq} = C_3.\frac{R_2}{R_1}$

3.2. Application as Inductor Simulator

The progress of integrated circuits has led to the design of synthetic inductances, which can be used instead of the bulky inductors. There are lots of recently proposed inductor simulators but the multifunctional metamutator, by properly terminating its ports, can act like a grounded or floating inductor with the advantage of simple circuitry as compared to the others.

According to Table1 connecting a capacitor and two resistors to three of the ports an inductor will be achieved at the fourth port with inductance value equal to the product of the three element values. Different realizations are shown in Table 3 and the simulation results will be given in the next section..

Table 3. Different inductor realizations

	Port 1	Port 2	Port 3	Port 4	Inductance Value
#1	L_{eq}	R_2	C_3	R_4	$sL_{eq} = \frac{R_2R_4}{\frac{1}{sC_3}} \rightarrow L_{eq} = C_3R_2R_4$
#2	R_1	L_{eq}	R_3	C_4	$sL_{eq} = \frac{R_1R_3}{\frac{1}{sC_4}} \rightarrow L_{eq} = C_4R_1R_3$
#3	C_1	R_2	L_{eq}	R_4	$sL_{eq} = \frac{R_2R_4}{\frac{1}{sC_1}} \rightarrow L_{eq} = C_1R_2R_4$
#4	R_1	C_2	R_3	L_{eq}	$sL_{eq} = \frac{R_1R_3}{\frac{1}{sC_2}} \rightarrow L_{eq} = C_2R_1R_3$

3.3. Application as FDNR Simulator

Low-pass filters are very important in radio frequency (RF) transceivers. The improvements in wireless communication have an increasing demand for reducing the size and improving the performance, cost of systems. In this process the much-used low-pass filter is called as anti-aliasing filter; Fig. 5 shows the position of anti-aliasing filter in digital radio receivers. [16]

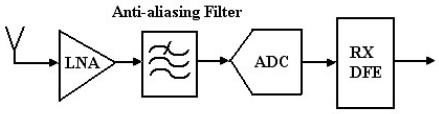

Fig. 5 Schematic of the digital radio receiver [16]

The anti-aliasing filter is a third or higher order passive LC ladder filter. Using an inductor in these circuits causes a lot of space use and reduces the performance. In order to reduce the size and to improve the performance one can use the FDNR [15] for designing a prototype of the LC ladder circuits which is explained in more detail in [16].

According to Table 1 replacing two capacitors and one resistor in three of the ports properly a grounded or floating FDNR will be achieved. Different realizations are shown in Table 4.

Table 4. Different realizations of FDNR

Realization	Port 1	Port 2	Port 3	Port 4	FDNR
#1	D_{eq}	C_2	R_3	C_4	$D_{eq} = \frac{1}{s^2 C_2 C_4 R_3}$
#2	C_1	D_{eq}	C_3	R_4	$D_{eq} = \frac{1}{s^2 C_1 C_3 R_4}$
#3	R_1	C_2	D_{eq}	C_4	$D_{eq} = \frac{1}{s^2 C_4 C_2 R_1}$
#4	C_1	R_2	C_3	D_{eq}	$D_{eq} = \frac{1}{s^2 C_3 C_1 R_2}$

4. Simulation Results

4.1. Memristor Realization

As the port description matrix of Metamutator with one active device is the same as recently proposed metamutators with two active devices all applications achieved by recently proposed two active device metamutators can also be obtained with only one active device Metamutator, by connecting proper elements to three ports of the Metamutator other circuit elements can be obtained at the fourth port [8,11]; a table similar to Table 2 in [8] can also be given for metamutator with FDCCII. For an illustration, by connecting an inductor to port 4, a capacitor and a nonlinear resistor $f_R(v_R, i_R) = 0$ to ports 2 and 3 respectively, as shown in Fig. 6, a memristor will be achieved at port 1.

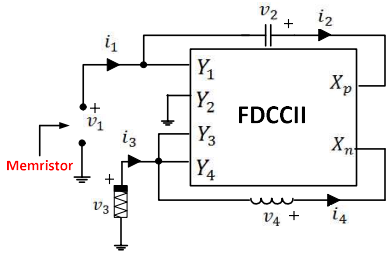

Fig. 6 Metamutator circuit mutating nonlinear resistor to memristor.

The metamutator circuit in Fig. 6 was simulated using a sinusoidal voltage source with amplitude of 4 V and frequency of 12 Hz at port 1. For the nonlinear resistor one diode 1N4148 and two resistors were used at port 3 of the metamutator. For FDCCII, TSMC 0.18 µm CMOS process parameters were used, with transistor dimensions as shown in Table 5 and its circuit in Fig. 7. The supply voltage is chosen as ±0.9V, $\boldsymbol{I_B}$ and $\boldsymbol{I_{SB}}$ as 50µA and, V_{bp} and V_{bn} as 0V. The inductor and capacitor values were selected as 10 nH and 0.4 mF, respectively.

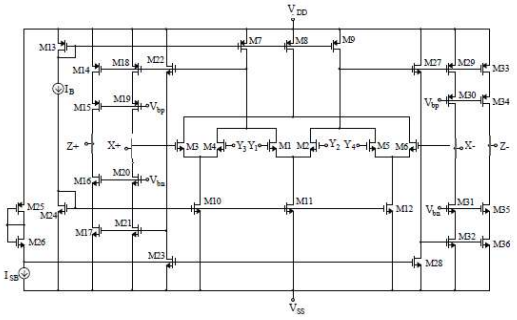

Fig. 7 The implementation of FDCCII [14]

The result of the simulation is shown in Fig. 8 with the Lissajou curve confirming the memristive relationship between v and i.

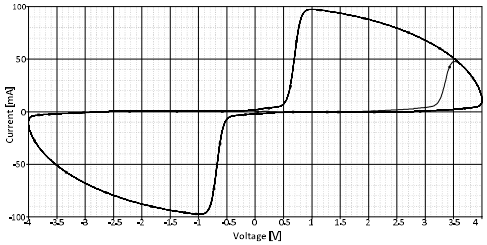

Fig. 8 $v - i$ characteristic of memristor

Table 5. Dimension of the transistors used in FDCCII

Transistors	W/L(µm)
$M_1, M_2, M_3, M_4, M_5, M_6$	8.75µm /0.7 µm
M_7, M_8, M_9, M_{13}	70µm /0.7 µm
$M_{10}, M_{11}, M_{12}, M_{24}$	17.5µm /0.7 µm
$M_{14}, M_{15}, M_{18}, M_{19}, M_{25}, M_{29}, M_{30}, M_{33}, M_{34}$	35µm /0.35 µm
$M_{16}, M_{17}, M_{20}, M_{21}, M_{26}, M_{31}, M_{32}, M_{35}, M_{36}$	8.75µm/0.35 µm
$M_{22}, M_{23}, M_{27}, M_{28}$	0.7µm /0.7 µm

4.2. Capacitance Multiplier Realization

Applying realization #2 in Table 2, the simulation results of the capacitor so obtained is demonstrated with Fig. 9.

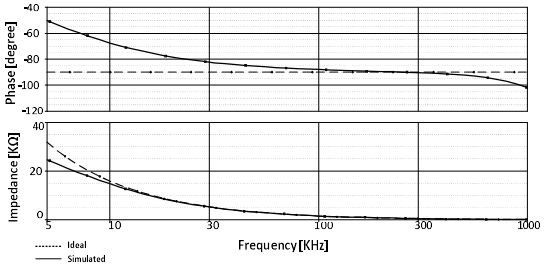

Fig. 9 Amplitude and phase of scaled capacitor in frequency domain

In this case the metamutator was simulated using an AC voltage source with amplitude 0.5 V. For FDCCII TSMC 0.18 µm CMOS process parameters are used with transistor dimensions as shown in Table 5 and the circuit in Fig. 7. The supply voltage is chosen ±0.9V, I_B and I_{SB} 50µA and V_{bp} and V_{bn} 0 V. Capacitor and resistor values are selected as 1 nF and 1kΩ, respectively

4.3. Inductor Simulator Realization

Applying realization #4 in Table 3 by placing two resistors and one capacitor in three of the ports of the metamutator, simulation results of the so obtained inductor are shown below with Fig. 10.

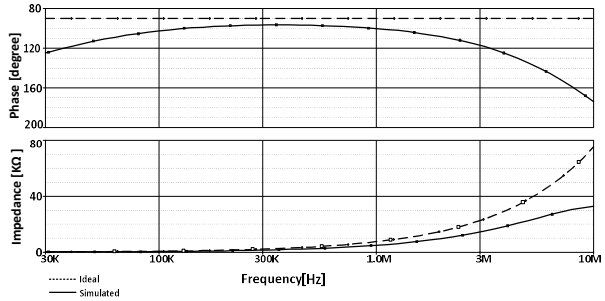

Fig. 10 Amplitude and phase of simulated inductor in frequency domain

In this case the metamutator was simulated using an AC voltage source with amplitude of 0.5V, for FDCCII TSMC 0.18 µm CMOS process parameters were used, with transistor dimensions as shown in Table 5 and its circuit in Fig. 7. The supply voltage is chosen as ±0.9V, I_B and I_{SB} as 50µA and V_{bp} and V_{bn} as 0V. The capacitor and resistors values are selected as 1 nF and 1kΩ, respectively

4.4. FDNR Realization

According to realization #4 in Table 4, connecting two capacitors and one resistor to three of the ports of the metamutator a FDNR will be observed from the fourth port**.** The simulation results are demonstrated below with Fig.11.

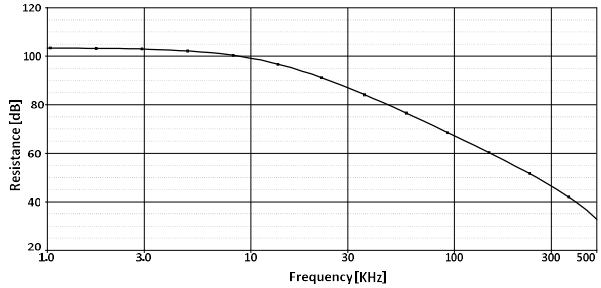

Fig. 11 Frequency domain characteristic of FDNR

In this case the metamutator was simulated using an AC voltage source with amplitude of 0.5V, for FDCCII TSMC 0.18 µm CMOS process parameters were used, with transistor dimensions as shown in Table 5 and its circuit in Fig. 7. The supply voltage is chosen as ±0.9V, I_B and I_{SB} as 50µA and V_{bp} and V_{bn} as 0V. The capacitor and resistor values are selected as 1 nF and 1kΩ, respectively.

6. Conclusions

Using only FDCCII as a single active device and no passive elements, the Metamutator is given a new realization which has been applied to capacitance scaling and memristor, inductor, simulation and FDNR realization. Depending on the choice of the input port, these realizations can be made grounded or floating. All four applications have been simulated with TSMC 0.18µm CMOS process parameters and shown to be in good agreement with theoretical results.

Future work will concentrate on building filters with FDNRs realized here and comparing the effect of using different kind of metamutators in the design of these filters.

7. References

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