A LOW POWER MOSFET-C FILTER FOR LOW FREQUENCY APPLICATIONS WITH POLYNOMIAL REGRESSIVE DESIGN

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Abstract

In this work, a novel current mode MOSFET-C filter is proposed for a wide range of low frequency applications from biomedical signal sensing up to speech processing region. Presented filter consumes only 2.3µW under 1V supply voltage. Besides, proposed filter is given with novel design methodology based on polynomial regressive small signal models. In this way, promising interaction between design parameters such as V_{GS} , V_{DS} , channel width (W) and channel length (L) and filter specs such as f_0 , Q and power is provided. Simulation results in 0.18µm CMOS technology are given and proposed filter is tested to process a real fetal PCG signal. It is shown that proposed filter attains a promising performance in comparison with the previously presented counterparts for low frequency applications.

1. Introduction

In the last decades, low frequency filters have a rising attention for biomedical signal sensing applications in order to process a wide range of signals such as Electrocardiogram (ECG), Electromyographic (EMC) or Phonocardiographic signals (PCG). Besides, audio frequency region has attained great deal of interest with rapidly growing of speech processing applications in smart phones, computers and wireless gadgets widespread in everywhere. Although a large numbers of studies are proposed to cover the huge demand in the market of low frequency operation, there are several limitations over circuit performances in analog design such as power consumption, supply voltage levels and bandwidth restriction. In this regard, some biomedical filters are proposed with reduced power consumption by employing active blocks such as op-amp or trans-conductance blocks etc [1-3]. Besides, [4] presents a flipped voltage follower structure under 0.6V power supply for the low frequency operations in voltage mode. Whereas a fourth order bandpass filter operated below 1kHz is proposed in [5], [6] brings a competitive solution in order to reduce supply voltage as low as 0.4V by means of using Dynamic Threshold Voltage MOSFET (DTMOS) and Voltage Differencing Trans-conductance Amplifier (VDTA)'s as active elements.

Some filters in current mode are presented in [7-9] using active blocks in order to get much higher bandwidth than voltage mode alternatives. [8] realizes companding filters in order to catch large time constants by employing active blocks of inductance and capacitor emulators. [9] proposes another DTMOS topology with a low power CCII block. In this respect, a novel current mode MOSFET-C filter is presented and it is easily tunable from 300Hz and 6.5 kHz approximately. Proposed filter makes use of external capacitances valued between 5pF and 6nF in order to realize the tuning mechanism. In order to prove the comparable performance of the presented filter structure, filtered output is given under a real PCG signal at 356 Hz. Furthermore, proposed current generator under 1V power supply brings promising compensation in order to avoid drastically changes with regard to temperature in the subthreshold region.

Moreover, a design methodology based on polynomial regression is presented in this study. It enables a good interaction between basic design parameters and design specs to prevent from a chain of hand calculations and computational burden. The produced polynomial regressive models of small signal parameters such as g_m , g_{ds} , C_{gb} and I_{DS} in subthreshold region are added into the automation algorithm presented in [10-12]. It reduces designer intervention when filter specs are satisfied in the end of design cycles.

The reminder of the paper is as follows: The next section describes proposed filter structure with aforementioned design methodology. Section.3 presents simulation results in the comprehensively analyses and comparison with the previously proposed works. Section.4 concludes the paper.

2. Proposed MOSFET-C Filter with Subthreshold Design Methodology

The proposed circuit is given in Fig.1 with the current generator. Core circuit consists of transistors operated in subthreshold region. In this region, C_{gb} dominates to the other capacitances and plays a critical role in the center frequency and quality factor of the filter. For properly dimensioning and operating in saturation region of the subthreshold design (i.e. $V_{DS} \geq 3\phi_t$ and $\phi_t = \frac{kT}{q}$) the following transfer functions can be obtained:

$$\frac{I_{BP}}{I_{in}} = \frac{s(C_{gb2}+C_2)g_{m1}}{s^2(C_{gb2}+C_2)(C_{gb1}+C_1)+s(C_{gb2}+C_2)g_{m1}+g_{m1}g_{m2}} \quad (1)$$

$$\frac{I_{LP}}{I_{in}} = -\frac{g_{m1}g_{m2}}{s^2(C_{gb2}+C_2)(C_{gb1}+C_1)+s(C_{gb2}+C_2)g_{m1}+g_{m1}g_{m2}} \quad (2)$$

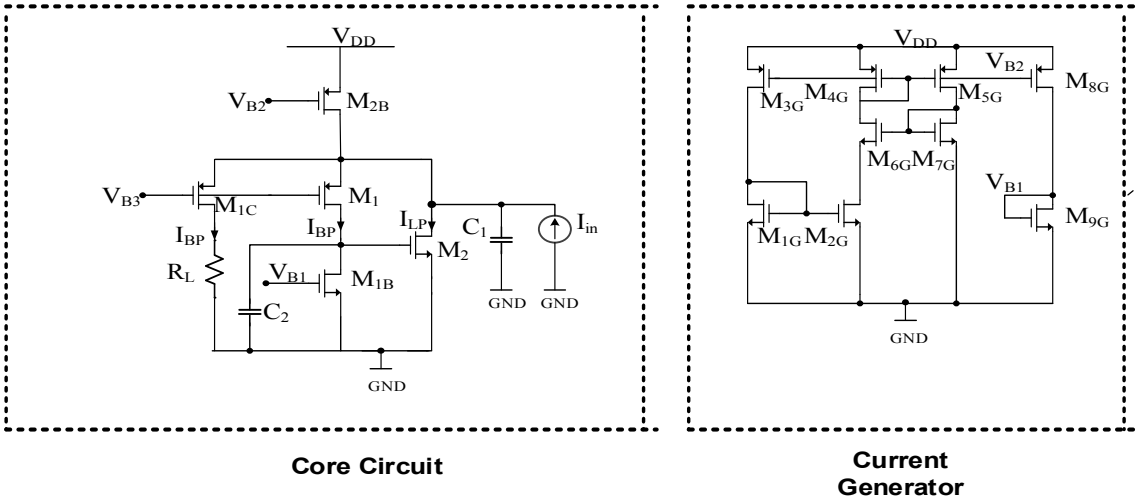


Fig.1 Proposed current mode tunable MOSFET-C filter for a wide range of low frequency operations

Where center frequency and quality factor are defined as follows:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{(C_{gb1}+C_1)(C_{gb2}+C_2)}} \quad , \quad Q = \sqrt{\frac{(C_{gb1}+C_1)g_{m2}}{(C_{gb2}+C_2)g_{m1}}} \qquad (3)$$

Current generator in the proposed filter is given in [13] brings a promising temperature compensation to the core circuit when M_{6G} and M_{7G} operates in deep subthreshold region whereas M_{1G} is biased in strong inversion and M_{2G} in triode. When g_m and C_{gb} 's of the copying transistor as M_{1C} and r_{ds} of the main transistors as M_1 and M_2 are taken into consideration, non-ideal ω_0 and Q can be described as follows:

$$\omega_0 = \sqrt{\frac{R_{ds2}g_{m2} + R_{ds2}g_{m1C} + R_{ds1}R_{ds2}g_{m1}g_{m2} + 1}{R_{ds1}R_{ds2}(\mathrm{C}_2+\mathrm{C}_{\mathrm{gb2}})(\mathrm{C}_1+\mathrm{C}_{\mathrm{gb1}}+\mathrm{C}_{\mathrm{gb1C}})}} \qquad (4)$$

$$Q = \sqrt{\frac{\left(R_{ds1}R_{ds2}(\mathrm{C}_2+\mathrm{C}_{\mathrm{gb2}})(\mathrm{C}_1+\mathrm{C}_{\mathrm{gb1}}+\mathrm{C}_{\mathrm{gb1C}})\right)}{\left(R_{ds2}g_{m2}+R_{ds2}g_{m1C}+R_{ds1}R_{ds2}g_{m1}g_{m2}+1\right)}}{\left(\begin{array}{l}R_{ds2}(\mathrm{C}_1+\mathrm{C}_{\mathrm{gb1}}+\mathrm{C}_{\mathrm{gb1C}}+\mathrm{C}_2+\mathrm{C}_{\mathrm{gb2}})+R_{ds1}(\mathrm{C}_2+\mathrm{C}_{\mathrm{gb2}})\\ +R_{ds1}R_{ds2}(\mathrm{C}_2+\mathrm{C}_{\mathrm{gb2}})(g_{m1}+g_{mC1})\end{array}\right)^2}} \qquad (5)$$

In this respect, a novel design methodology based on polynomial regression is given in order to allow these non-ideal functions to convert the ideal ones in (3) by means of using direct interaction between design specs and fundamental design parameters such as bias voltages or currents and aspect ratios. Fundamentals of the design algorithm are summarized in [10-12]. This algorithm automates the filter design based on MOSFET-Only or MOSFET-C structures in order to cover design specifications. In this work, conventional small signal definitions in subthreshold region are converted to the functions of bias voltages and aspect ratios in a good approximation for 0.18µm TSMC CMOS technology. Conventional ones based on technological parameters, which are kept as confidential metrics by vendors and roughly mathematical expressions bring huge computational error and a chain of hand calculations increasing design time. In the subthreshold region, g_m , C_{gb} and g_{ds} are defined as follows:

$$g_m \approx \frac{I_{DS}}{n\phi_t} \ , \ C_{gb} \approx WLC_{ox} \qquad (6)$$

$$g_{ds} \approx \eta g_m \qquad (7)$$

where $\phi_t = \frac{kT}{q}$, n and η represents subthreshold slope factor and drain induced barrier lowering coefficient (DIBL) respectively [14,15]. As shown in Fig.2, g_m is reconstructed for a wide range of channel length and bias voltage as follows:

$$g_m = W * \begin{pmatrix} t_{i1} + t_{i2}L + t_{i3}V_{GS} + t_{i4}L^2 + t_{i5}LV_{GS} + t_{i6}{V_{GS}}^2 + t_{i7}L^3 \\ + t_{i8}L^2V_{GS} + t_{i9}L{V_{GS}}^2 + t_{i10}{V_{GS}}^3 + t_{i11}L^4 + t_{i12}L^3V_{GS} \\ + t_{i13}L^2{V_{GS}}^2 + t_{i14}L{V_{GS}}^3 + t_{i15}{V_{GS}}^4 \end{pmatrix} \qquad (7)$$

$$\left\{\begin{array}{l} a = \mathrm{linspace}(0.1, 1.8, 5) \\ a(\mathrm{k}) < \mathrm{V_{DS}}(\mathrm{k}) \le a(\mathrm{k}+1) \\ \mathrm{k} \in [1,4]\ ,\ i \in [1,4], L \in [1,10],\ W \in [2,600]\ \mu m \end{array}\right\} \qquad (8)$$

In this regression, g_m is piece-wise reconstructed in order to take variations of V_{DS} voltage into account and 1000 CADENCE-SPECTRE data are processed. Meanwhile, for overall polynomial regressive models, it is necessary to note that channel length of the devices in subthreshold region should be equal or bigger than 1µm in order to avoid parasitic drain capacitance dominating effects [14]. Furthermore, bulk and source terminals should be shorted and V_{DS} voltage must be bigger than 26mV to operate in saturation region of the subthreshold operation [14,15]. In the end of regression, $'t'$s are coefficients in different units and can be changed with regard to transistor type.

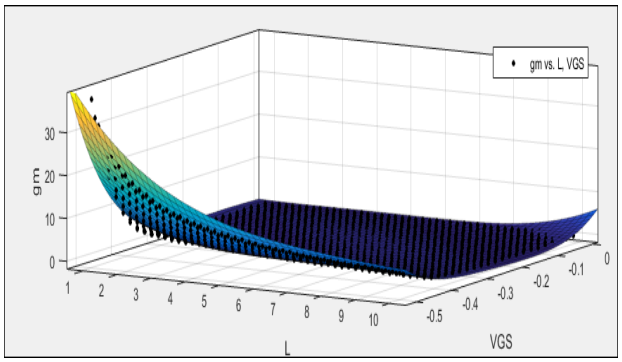


Fig.2 g_m (in µS) variation of PMOS device versus channel length and V_{GS} voltage (L is between 1µm and 10 µm, whereas V_{GS} changes between 10mV and 0.5V. Colored surface is polynomial surface, dots represent fitted simulation data.)

In the same way, g_{ds} is modelled with piece-wise regression in order to take into consideration channel length effect as follows:

$$g_{ds}=W*\begin{pmatrix} w_{i1}+w_{i2}V_{GS}+w_{i3}V_{DS}+w_{i4}{V_{GS}}^2+w_{i5}V_{GS}V_{DS}+w_{i6}{V_{DS}}^2+ \\ w_{i7}{V_{GS}}^3+w_{i8}{V_{GS}}^2V_{DS}+w_{i9}V_{GS}{V_{DS}}^2+w_{i10}{V_{DS}}^3+w_{i11}{V_{GS}}^4 \\ +w_{i12}{V_{GS}}^3V_{DS}+w_{i13}{V_{GS}}^2{V_{DS}}^2+w_{i14}V_{GS}{V_{DS}}^3+w_{i15}{V_{DS}}^4 \end{pmatrix} \quad (9)$$

$$\left.\begin{matrix} b=\text{linspace}(1,10,11)\ ,\ b(\text{i})<L(\text{i})\le b(\text{i+1}) \\ L\in[1,10],\ W\in[2,600]\ \mu m\ \ i\in[1,10] \end{matrix}\right\} (10)$$

(9) and (10) brings direct relationship between design specs and bias voltages and dimensions for output transconductance, where 'w's are multipliers in different units. Another important small signal parameter is gate-bulk capacitance can be modelled in the following form:

$$C_{gb}=0.85*W*\begin{pmatrix} p_1+p_1L+p_2V_{GS}+p_3LV_{GS}+p_4{V_{GS}}^2+p_5L{V_{GS}}^2 \\ +p_6{V_{GS}}^3+p_7L{V_{GS}}^3+p_8{V_{GS}}^4 \end{pmatrix} (11)$$

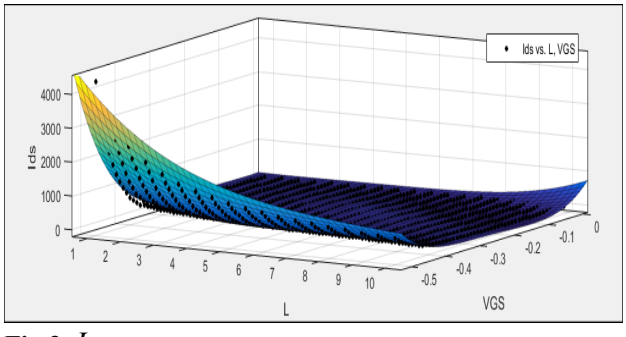


Fig.3 I_{DS} (in nA) variation of PMOS device versus channel length and V_{GS} voltage (L is between 1µm and 10 µm, whereas V_{GS} changes between 10mV and 0.5V. Colored surface is polynomial surface, dots represent fitted simulation data.)

Furthermore, subthreshold current is roughly approximated in saturation region of the weak inversion as follows:

$$I_{DS}\approx I_0 e^{\frac{V_{GS}-V_t}{n\phi_t}},\ I_0\approx\mu_n C_{ox}\frac{W}{L}(\text{n}-1)\phi_t^2 \quad (12)$$

In this respect, I_{DS} should be reconstructed by means of piece-wise polynomial regression with regard to V_{DS}. Aforementioned direct relationship between design specs and design parameters makes use of the following model as shown in Fig.3:

$$I_{DS}=W*\begin{pmatrix} m_{i1}+m_{i2}L+m_{i3}V_{GS}+m_{i4}L^2+m_{i5}LV_{GS}+m_{i6}{V_{GS}}^2 \\ +m_{i7}L^3+m_{i8}L^2V_{GS}+m_{i9}L{V_{GS}}^2+m_{i10}{V_{GS}}^3+m_{i11}L^4+m_{i12}L^3V_{GS} \\ +m_{i13}L^2{V_{GS}}^2+m_{i14}L{V_{GS}}^3+m_{i15}{V_{GS}}^4+m_{i16}L^5+m_{i17}L^4V_{GS}+m_{i18}L^3{V_{GS}}^2 \\ +m_{i19}L^2{V_{GS}}^3+m_{i20}L{V_{GS}}^4 \end{pmatrix} (13)$$

$$\left.\begin{matrix} c=\text{linspace}(0.1,1.8,5) \\ c(\text{k})<\text{V}_{\text{DS}}(\text{k})\le c(\text{k+1}) \\ \text{k}\in[1,4]\ ,\ i\in[1,4], L\in[1,10],\ W\in[2,600]\ \mu m \end{matrix}\right\} (14)$$

In this regard, dominant small signal parameters in subthreshold region and DC current can be expressed in terms of bias voltages and aspect ratios with direct interaction. Automation algorithm in [10] takes the aforementioned polynomial regression models and targets to match predefined design specs. In this work, core circuit with the current generator is dimensioned as tabulated in Table.1.

Table 1. Proposed low frequency filter design with polynomial regressive models

Device Specs (Design 1)	Cadence-SPECTRE	This Work (Polynomial Regression)
f_0 > 200Hz	371Hz	354Hz
Q > 0.8	0,81	0.82
Power < 3µW	2.3µW	2.18µW
Aspect Ratios (With Bias Voltages)	M_1 W=4µ, L=1µ M_{1C} W=50µ, L=1µ M_{1B} W=15µ, L=5µ C1=6nF, C2=250pF Current Generator_Dimensions: M_{1G} W=7µ, L=4µ M_{3G} W=10µ, L=3µ M_{5G} W=10µ, L=10µ M_{7G} W=45µ, L=2µ M_{9G} W=20µ, L=5u	M_2 W=3µ, L=3µ M_{1B} W=5µ, L=5µ V_{B3}=0.5V M_{2G} W=7µ, L=4µ M_{4G} W=15µ, L=10µ M_{6G} W=180µ, L=2µ M_{8G} W=5µ, L=3µ V_{DD}=1V, R_L=1k

3. Simulation Results

In order to prove the performance of the proposed filter structure with aforementioned design technique, CADENCE-SPECTRE is used with 0.18µm TSMC CMOS technology. In the simulations, BP output is observed and tunability of the output with external capacitors is shown for a wide range of low frequency applications.

As observed in Fig.1, BP output stays at 371 Hz and reconfigurable with the external capacitances. Furthermore, poly regressive model based estimation with detailed expressions in (4) and (5) is very close to the simulator result. As shown in Fig.5, center frequency of the filter can be easily tuned by external two capacitors. In the first case, f_0 is between 300Hz and 1.8kHz approximately, whereas Q changes from 0.6 up to 3. The second case as shown in b), f_0 is between 1.87kHz and 6.35kHz approximately, whilst Q changes from 0.8 up to 3.

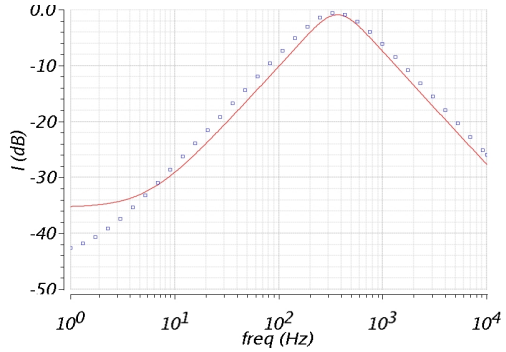


Fig.4 BP output at 371 Hz. (Blue dots represent poly regressive model estimation, red one shows CADENCE-SPECTRE result.)

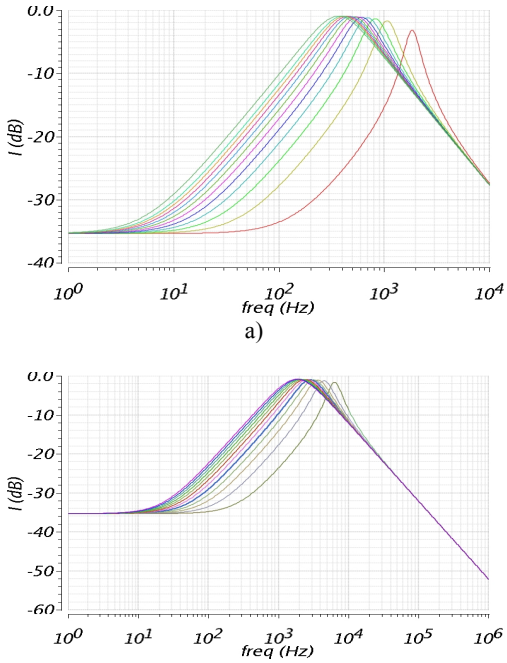


Fig.5 BP output tuning. (a) C1 is 6nF, C2 changes from 10pF up to 250pF. b) C1 is 1nF, C2 changes from 5pF up to 60pF.)

Proposed filter proves its performance with regard to different conditions as observed in Fig.6. Furthermore, Monte-Carlo simulation is performed by taking into account mismatches and process variations. In the end of MC, center frequency stays in acceptable limits with 365Hz mean and 7.5% standard deviation. Moreover, extremely temperature variation brings up to 5% variation to the frequency response due to the temperature compensated current generator.

A real biomedical signal is obtained from [16] shows the characteristic of the proposed BP filter's promising performance. Real PCG signal at 356Hz is applied to the input of filter with undesired parts at lower frequencies as shown in Fig.7a. Filtered signal between 6.s and 9.s can be shown in Fig.7b and it is achieved to catch targeted parts by eliminating the other parts. At the end of this part, it is seen that proposed filter presents a competitive performance by taking into consideration Figure of Merit (FOM) in (15) as compared in Table.2.

$$FoM = \frac{P\,x\,V_{DD}}{n\,x\,f_c\,x\,DR} \quad (15)$$

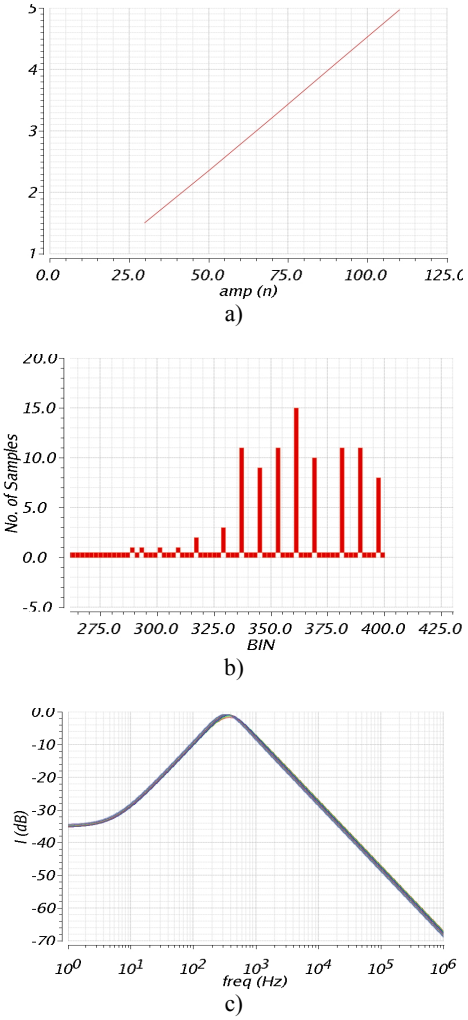
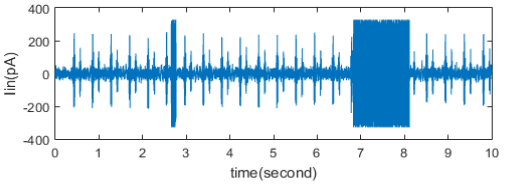
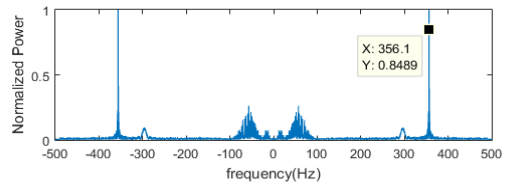
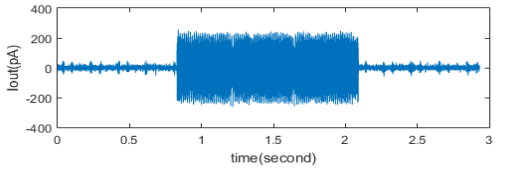


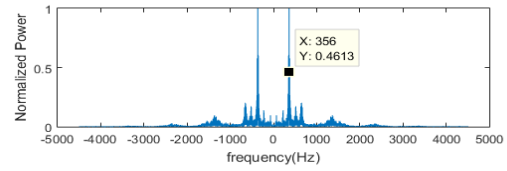
Fig.6 Proposed filter's performance measurement (a) THD performance with regard to input current from $60nA_{p\text{-}p}$ up to $220nA_{p\text{-}p}$, b) MC simulation for 100 random MC points, c) BP output changing with temperature deviation from -25^0C up to 105^0C)





a)





b)

Fig.7 Real filtered fetal PCG signal. a) Input, b) Output with interval between 6th second and 9th second.

Table 2. Proposed filter's performance in comparison with the other topologies.

Filter Specs	[1]	[2]	[5]	[6]	[8]	This Work
Supply(V)	0.9	2.8	1	±0.2	0.5	1
Power(nW)	262k	230	14.4	12.7	16.19	2.3k
DR(dB)	52	67.5	55	63.7	55.24	60
fc(Hz)	1.12k	141	732	19.5	6	300-6.5k
Order(n)	6	4	4	4	2	2
THD(%)	1	5	1	2	-	2
FoM(10^{-13})	6632	169	0.89	10.2	122	95.8

6. Conclusions

In this work, a novel low power MOSFET-C filter is presented for low frequency operations. Proposed structure can be easily tuned from biomedical signal sensing operations up to speech processing applications. It should be note that developed new reformulations of the small signal parameters based on polynomial regression make the design of the subthreshold filters very easier and decreases computational burden with reduced user intervention. It comes from the fact that design parameters and specs are connected between each other's by using piece-wise regression with high accuracy. Simulation results prove the competitive performance of the proposed filter and design technique as well.

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7. References

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