Impact of Transistor Scaling on the Time-Dependent Dielectric Breakdown (TDDB) Reliability of Analog Circuits

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Abstract

This paper discusses the dielectric breakdown reliability of a two-stage operational amplifier across four short-channel device technologies. For a long time, time dependent dielectric breakdown (TDDB) impact was only confined to digital circuits as the electric field across the gate oxide is relatively large despite being applied in accordance with the activity factor. However, in analog circuits, electric field is generally smaller, though it is constant. One particular aspect that was of interest is the change in TDDB reliability of analog circuits when the device technology descends into deep nanoscale regime. This paper shows that the amplifier reliability becomes mostly enhanced as the transistor technology scales down from 90nm to 32 nm.

1. Introduction

As electronic systems scale down in size, their power consumption has become more important. Reduction of power supply voltage is one of the most popular approaches to reduce the power consumption [1]. As power supplies scale down, gate oxide thicknesses will decrease to be able to work in that low voltage regime. In modern CMOS very large scale integrated (VLSI) circuits, thin oxide transistors are commonly used in digital circuits. It was shown that digital circuits can be impaired at varying levels due to dielectric degradation [2]. Recent studies revealed that the gate-oxide reliability of a circuit is also critical in analog and mixed-signal circuit designs [3], [4]. Although the TDDB reliability of analog and RF circuits has been explored as well [5], studies of circuit reliability have been generally confined to digital circuits.

Today, most designs are composed of both digital and analog blocks. Thus, the reliability of the circuit performance should be analyzed thoroughly considering both types. There are several modeling and simulation approaches to analyze the circuit reliability [6]. This paper will mainly focus on the time-dependent dielectric breakdown (TDDB) impact on CMOS two-stage operational amplifiers designed in different transistor technologies ranging from 90 nm to 32 nm. Section 2 reviews the theoretical background of TDDB. Section 3 discuses the models to analyze the gate-oxide reliability. Section 4 presents the results of the performed analysis and simulation results. Section 5 summarizes the conclusions of the paper.

2. Time-Dependent Dielectric Breakdown

Reduction of device sizes and supply voltages to attain better integration and lower power consumption, has been a problem for the last few decades. Downscaling not only made the devices to have more leakage current but also more vulnerable to TDDB. Over the years, reliability of CMOS devices has been deeply explored, nevertheless several questions remained open [7]. One of those is regarding the voltage dependence of the time-to-breakdown (T_{BD}) or charge-to-breakdown (Q_{BD}) since the device lifetime expectancy and the oxide reliability can change greatly with respect to this dependence. Even though, there are several dielectric breakdown models based on impact ionization, hydrogen release, anode hole injection, and field-enhanced bond breakage, there is no agreement on which model is the most realistic and accurate. Robustness to TDDB can be quantified by the time scale for which the dielectric can keep its high electrical resistivity under external stress. TDDB stress test is done by putting the dielectric between two electrodes, thereby applying a stress voltage under high temperature [8]. The leakage current is then analysed as a function of stress time. The duration in which the leakage current reaches a predetermined critical value is called the dielectric lifetime under stress condition. However, under nominal operating conditions, time-to-breakdown would take years. Therefore, experiments are done in accelerated conditions. Accelerated tests are conducted at an elevated temperature and a larger electric field than the device would have normally observed in typical working conditions. Then, the obtained data is extrapolated based on the typical operating conditions to estimate the TDDB degradation time of the transistor under test. In order to yield successful results, experiments and modeling should be done with a good understanding of the dielectric breakdown mechanism. There are two modes of TDDB called intrinsic and extrinsic breakdown which will be individually discussed in the next two sections.

2.1. Intrinsic Breakdown

TDDB happens to be near or at the interface of the dielectric and the metal of a transistor. When there is no metal contamination in the dielectric interface, the breakdown is caused by the intrinsic breakdown. Intrinsic breakdown was the main issue in integrated circuit (IC) applications from 1970s to 1990s. In that period, ICs were built using aluminum. SiO_2 can react with Al, which forms stoichiometric Al_2O_3, that creates a barrier for metal penetration in SiO_2. This would make more stable interfaces, thus the main cause of the dielectric failure would be intrinsic SiO_2 breakdown.

The intrinsic breakdown is related to the defect generation during carrier injection damage in stress. These are closely related with the chemical compound of the dielectric and the type of leakage current transportation. There are several models to analyze intrinsic breakdown mechanism. These models are used to predict lifetime of devices under stress, which gives a prediction for lifetime under normal conditions. These models will be discussed in section 3.

2.2. Extrinsic Breakdown

When copper replaced aluminum as the interconnect metal in 1990s, the aim of the TDDB research changed to extrinsic breakdown. Several studies claimed that the dielectric reliability is related to the metal contamination, such as Cu [9]. If Cu occupancy is increased, the lifetime will shorten dramatically. However, by taking proper precautions, the risk of extrinsic breakdown can be significantly reduced.

3. Lifetime Analysis Models

In this section several models for TDDB degradation will be described which are critical to estimate the TDDB lifetime.

3.1. Thermochemical Model

Thermochemical model, also known as the E model, is developed by McPherson and Baglee [10]. It is widely used to explain the internal dielectric breakdown. This model suggests that the defect generation is not based on the leakage current in the oxide, rather it is a field-driven process [6]. The main idea states that the conductive percolation path is arisen between anode and cathode under stress [8]. Broken $Si - O$ bonds created due stress form these percolation paths, therefore the dielectric lifetime is affected by the bond-breakage rate. The dielectric is polarized and a dipole field is formed under the electric field E_0. The effective electric field, combination of the E_0 and the dipole field, creates a stress on the highly polar $Si - O$ bonds, where the electric field and the dipole field are aligned. Bonds will eventually breakdown when the electric field becomes large enough. Even though, the electric field is not sufficient to break the bonds, the stress will lower the barrier of bond breakage. Heat variations will accelerate the bond breakage process due to barrier lowering. Furthermore, thermal fluctuations can also speed up the breakdown process through carrier injection. The E model-based time-to-breakdown is

$$ln(T_{BD}) \propto \frac{\Delta H_0}{k_B T} - \gamma E_0, \tag{1}$$

where ΔH_0 is the activation energy of the bond breakage, T is the temperature and γ is the field acceleration parameter related to the dipole polarization.

One of the problems of E model is that it does not explain the polarity dependence [10]. If the roles of anode and cathode is changed TDDB effect will be altered as well.

3.2. Anode Injection Model

Anode injection model (AHI), also known as $1/E$ model, is a current based TDDB degradation model [10]. If an increased amount of current flows through any material (insulator or conductor), the device will fail at a critical breakdown current (J_{crit}) due to large Joule-heating effects. This model is based on the impact of the Fowler-Nordheim (FN) tunneling current t the dielectric. Electrons injected from the cathode are accelerated toward the anode thereby damaging the dielectric due to impact ionization. Holes created near the anode can tunnel back to the dielectric, which also causes additional damage. The time-to-breakdown (TDDB) formula is,

$$T_{BD} = \tau_0(T) \cdot \exp\left[\frac{G(T)}{E_{ox}}\right], \tag{2}$$

where $G = B + H$, with B being related to the electron tunneling and H being related to the hole tunneling, $\tau_0(T)$ is the temperature dependent parameter. Usually, Q_{BD} is used to express the reliability of the device $1/E$ model. However, under 5 nm oxide thickness, its importance is reduced.

There are two concerns regarding this model: First, the hole production is extremely low in small fields. Second, production of defects by injecting holes in the silica is not efficient enough. The strong temperature dependence cannot be properly explained as well, since the FN tunneling is not strongly temperature dependent.

3.3. Anode Hydrogen Release Model

Anode hydrogen release model (AHR), also known as the power-law voltage model, is based on the assumption that $Si - H$ bonds at the dielectric interface are excited by single (coherent) or multiple (incoherent) events of electron processes [10]. At the anode, such processes cause hydrogen to be discharged to silica bulk. The interaction between weak bonds in the silica and the released hydrogen supposedly lead to defect generation, formation of percolation paths, and finally to the breakdown event. The AHR model is initially designed for ultra thin dielectric. The power-law formula for ultra thin oxides is given as:

$$T_{BD} = B_0\left(T\right)\left(V^{-N}\right). \tag{3}$$

Here, N varies between 40 and 48. Even though AHR model is developed primarily for ultra thin oxides, it can be used with thicker oxides, as well.

The main concern for the AHR model is that the theory does not explain the temperature dependence of TDDB and the drop in activation energy with field. Moreover, the released hydrogen at the anode can cause breakdown, as oxide gets thicker which could be reduced. However, thicker oxides still show reliability problems.

3.4. $\sqrt{E}$ Model

$\sqrt{E}$ model is developed for low-k silicon based interconnect devices [10]. Current induced oxide breakdown models assume that the breakdown event is caused by the current flowing through the dielectric. The current flow usually has a FN tunneling nature for high quality oxide, thus $1/E$ model is used. Nonetheless, the current flow for low quality oxides, or dielectric types, may be similar to Poole-Frenkel or Schottky conduction. So, for these types of dielectrics the time-to-breakdown model for TDDB is formulated as

$$T_{BD} = D \cdot exp\left(\frac{Q_{bh} - \lambda\sqrt{E}}{k_B T}\right), \tag{4}$$

where λ is the root field accelerator, and Q_{bh} is the barrier height. As with other models, $\sqrt{E}$ model cannot well explain the strong temperature dependence [10].

4. Case Study: TDDB Analysis of a Two-Stage Operational Amplifier

4.1. Design of a Two-Stage Operational Amplifier

Operational amplifiers are one of the fundamental blocks in many analog circuits. To test their gate-oxide breakdown reliability, a two stage operational amplifier shown in Figure 1 has been choosen as a case study. The two-stage amplifier consists of a differential amplifier building the first stage (M1 - M2), a common-source amplifier acting as the second first stage (M7 - M8) and a biasing current mirror (M5 - M6). Even though,

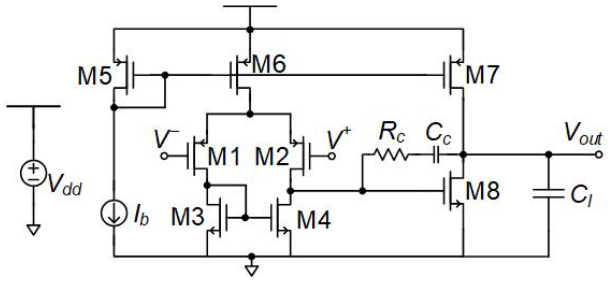

Figure 1. The schematic used for modeling the OPAMPs

similar analog circuits have been analyzed for TDDB reliability such as [1] and [3], none of them covered the changes of the reliability results when the same circuit is designed in different technology nodes.

The circuits for reliability tests are designed in 90 nm, 65 nm, 45 nm, and 32 nm bulk CMOS technologies from the Predictive Technology Library [11]. The operating voltage is 1.2 V. The input common-mode voltage of all amplifiers is 0.5 V. The gate-oxide thicknesses (t_{ox}) of n-type and p-type MOSFETs from different technologies are given in Table 1. All designs were done both with transistors of channel lengths (λ) with $2L_{min}$ and $3L_{min}$ for all technologies. The body terminals of PMOS and NMOS are connected to power supply voltage and ground respectively. The Miller-compensated capacitance C_2 is a metal-insulator-metal design, which has no effect on the gate-oxide breakdown. For all amplifiers, it is aimed that they have a 60 dB gain, 60° phase margin and 500 MHz unity-gain bandwidth.

Table 1. Gate oxide thickness values of device technologies employed

Technologies	NMOS (nm)	PMOS (nm)
32 nm	1.65	1.75
45 nm	1.75	1.85
65 nm	1.85	1.95
90 nm	2.05	2.15

The open-loop gain (A_V), unity-gain bandwidth (UGBW) and phase margin (PM) of the designed amplifiers are given in Table 2 with corresponding transistor channel lengths respectively. The load capacitance is set to 1 pF.

Table 2. Gain, phase margin, unity-gain bandwidth of the designed operational amplifiers

Tech.	λ	A_V (dB)	PM (°)	UGBW (MHz)
45-nm	$2l_{min}$	57.8781	60.386	528.566
65-nm	$2l_{min}$	60.0751	60.043	784.087
90-nm	$2l_{min}$	60.0295	60.188	729.144
32-nm	$3l_{min}$	60.1151	61.41	928.874
45-nm	$3l_{min}$	60.4322	60.009	1005.98
65-nm	$3l_{min}$	60.6293	61.214	922.551
90-nm	$3l_{min}$	60.2684	58.952	791.547

4.2. Modeling of TDDB Effects in Analog Circuits

Simulation model selection is an important part to investigate the gate-oxide breakdown effects. As discussed in the previous section, the design is affected by the silicon interface itself, so, the $\sqrt{E}$ model cannot be used for these circuits. E and $1/E$ models have to be directly applied on the circuit to get accurate results. These models have lots of experiment-based calculations which would be problematic for circuit simulation. Moreover, they do not clearly explain the post breakdown effects, which are important considering the impact of TDDB on circuit behavior. Linder et al. have proposed a simulation model which was best the fit for the circuit TDDB analysis simulations [12]. In this paper, simulations were done using a slightly modified version of that model. There, the post breakdown current has a dependence on voltage and oxide thickness,

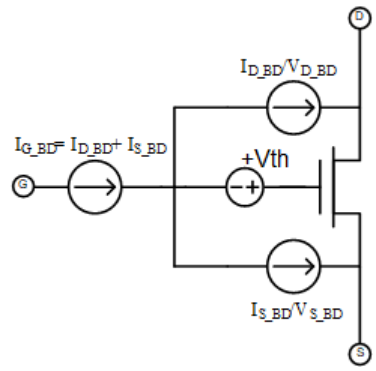

Figure 2. Current model representation

$$DR = k \cdot \exp\left(\frac{aV_G}{bt_{ox}}\right), \tag{5}$$

where DR is the defect current growth rate, V_G is the stress voltage and a, b are constants. In simulations, a and b are selected as 1 to reduce their impact on the results. The time-dependent post breakdown current can be shown as

$$I_{BD}(t) = I_0 \cdot \exp\left(\frac{t}{G_D}\right), \tag{6}$$

where I_0 is the the gate-current measured right after the soft-breakdown (SBD), G_D is the growth time parameter defined from I_0 to I_F (the current when the circuit fails). G_D is critical as it gives a measure of TDDB degradation on the designed amplifiers. G_D is expressed as:

$$G_D = \frac{I_F - I_0}{DR \cdot ln(10)}. \tag{7}$$

To guide the circuit design for TDDB reliability, gate leakage current should be modeled using ideal circuit elements. For this purpose, the model shown in Figure 2 is used. This model relies on the leakage currents flowing through the gate-drain and gate-source junctions. In simulation models, these resistances represent the defects in the oxide, which leads to the breakdown event.

The model analysis of the leakage currents is based on both drain and source sides. However, defects are often not evenly distributed. Most of the device failures are due to defects formed on one of the either sides [13]. Based on this assumption, reliability simulations are done for either source or drain leakage resistance of transistors. Furthermore, it is important to select which transistors are dominant to affect the TDDB

reliability. In simulations, it has been found out that for the two-stage operational amplifier, M4, M6, and M8 have the biggest impact.

4.3. Simulation Results

All reliability simulations concentrate on the the time scale at which the amplifier gain drops to 50% of its initial value due to reduced gate resistance near the drain end. Gain drop of 50% is considered to correspond to the hard dielectric breakdown of the transistors under test. Simulations are conducted for the drain side of M4, M6, and M8 transistors. Table 3, Table 4, and Table 5 show the breakdown times for these tests where time to 20%, 30%, 40%, and 50% gain drop is calculated with 10% gain drop is taken as the starting time of the device failure.

Table 3. TDDB Analysis of M4

Tech.	λ	20% (s)	30% (s)	40% (s)	50% (s)
45 nm	$2L_{min}$	101.46	153.02	184.82	207.48
65 nm	$2L_{min}$	36.83	65.44	86.95	101.44
90 nm	$2L_{min}$	51.37	79.40	97.69	110.14
32 nm	$3L_{min}$	75.23	179.64	299.28	406.76
45 nm	$3L_{min}$	41.39	97.92	155.10	199.79
65 nm	$3L_{min}$	41.10	90.96	136.24	168.46
90 nm	$3L_{min}$	1.63	2.39	2.75	2.94

Table 4. TDDB Analysis of M6

Tech.	λ	20% (s)	30% (s)	40% (s)	50% (s)
45 nm	$2L_{min}$	0.027	0.039	0.046	0.049
65 nm	$2L_{min}$	0.057	0.085	0.099	0.106
90 nm	$2L_{min}$	0.010	0.015	0.017	0.018
32 nm	$3L_{min}$	0.480	0.723	0.846	0.908
45 nm	$3L_{min}$	0.144	0.215	0.250	0.268
65 nm	$3L_{min}$	0.109	0.163	0.190	0.203
90 nm	$3L_{min}$	0.030	0.044	0.052	0.055

From Tables 3-5, it can be assumed that M6 affects the amplifier TDDB reliability at most. Nevertheless, gate resistances at which the breakdown time takes place corresponds to different dielectric breakdown ranges. M6 reaches to $\%50$ gain drop at a gate resistance around $1k\Omega$ - $10k\Omega$ range whereas M8 gets to the same gain drop around $10k\Omega$ - $1M\Omega$ resistance range.

Table 5. TDDB Analysis of M8

Tech.	λ	20% (s)	30% (s)	40% (s)	50% (s)
45 nm	$2L_{min}$	40.33	61.01	71.63	77.10
65 nm	$2L_{min}$	40.48	61.26	70.37	75.49
90 nm	$2L_{min}$	30.26	45.35	52.94	56.80
32 nm	$3L_{min}$	28.7	43.07	50.22	53.76
45 nm	$3L_{min}$	8.14	12.35	14.42	15.43
65 nm	$3L_{min}$	7.05	10.59	12.34	13.18
90 nm	$3L_{min}$	4.14	6.44	7.49	8.01

The results show that, generally, as technology gets smaller amplifiers become more robust to TDDB degradation. In short channel devices the transconductance becomes larger and the output resistance scales down. This in turn means that it takes more time for the gate leakage to become significant in terms of the drain current. From a different point of view, for short channel technologies, the gate resistance has to come down further in order to become comparable with the output resistances so that they can be considered as a leakage path. Simulation outcomes have been corraborated by the measurement results and it is validated that as the channel lengths are reduced the TDDB reliability of the transistors is enhanced [14], [15], [16]. However, for some devices in designs with $2L_{min}$ transistors, the TDDB reliability improvement can be very small. More specifically, as shown in Table 4, a longer channel technology (65 nm) can turn out to be more robust to TDDB degradation than a shorter channel technology (45 nm). This indicates that TDDB robustness at very short channel lengths does not obey the trend discussed in this paper and should be further investigated with more examples.

5. Conclusion

In this paper, the impact of TDDB on analog circuits has been investigated. A procedure to assess the TDDB reliability of an analog circuit based on a known TDDB simulation model is described and studied in the case of a two-stage operational amplifier. It is shown that the reliability analysis methodology applied here yields similar results as the measurements previously published, thereby confirming in general the increased reliability of analog circuits at nanoscale regime toward TDDB. As future work, the analysis described in this paper will focus on analog circuits that involve very short channel lengths and are primarily designed for high-frequency applications. The main aim of this effort will be to better explain the relationship between the channel length size and the robustness to TDDB degradation.

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