A Novel CMOS Constant-Bandwidth Variable-Gain Amplifier for WiMAX Receivers

Ali Doğuş Güngördü, Nil Tarim

Istanbul Technical University, Department of Electronics and Communication Engineering, Istanbul, Turkey
gungordua@itu.edu.tr, tarimn@itu.edu.tr

Abstract

In this study, a novel variable-gain amplifier (VGA) is proposed. A mathematical analysis of the circuit is given. The proposed circuit keeps a constant current flowing through the load transistors and provides a constant bandwidth over the voltage gain range. The circuit is designed with TSMC 180 nm CMOS technology, using 1.8 V single supply voltage and simulated with Cadence Analog Virtuoso.

1. Introduction

The variable-gain amplifier (VGA) is an indispensable building block to maximize the dynamic range of wireless communication links, where the amount of variation in the received signal strength is significant due to channel fading [1]. The variable-gain function can be realized in discrete or continuous form. Orthogonal frequency-division multiple access systems (OFDMA) or wideband code-division multiple access (WCDMA) transmitters require a continuous gain control to provide high peak-to-average power ratio (PAPR) and to avoid signal phase discontinuities [2, 3]. The gain control function should have an exponential relationship (or linear-in-dB) so that the automatic gain control (AGC) system, in which VGAs are usually used, provides a constant settling time [4]. There are many ways to implement a linear-in-dB CMOS VGA such as using a pseudo-exponential function [5] or Taylor series expansion [6]. Pseudo-exponential functions are usually implemented using a g_m-ratioed amplifier, whose gain is defined by the ratio of the input and load transconductances [5]. Since the load changes with varying gain, the bandwidth of the circuit changes as well for both the Taylor series expansion and the pseudo-exponential function, which makes it difficult to optimize the speed of the AGC system.

This paper is focused on the VGA core rather than the exponential control generation. In section 2, we provide a mathematical description of the proposed VGA. In section 3, the design flow is described for required noise and linearity performance. In section 4, we present simulation results to demonstrate the circuit performance. Finally, section 5 draws the conclusion.

2. Circuit Description and Analysis

The proposed VGA is based on the Gilbert cell, as shown in Fig. 1. The idea is to use the cell for adding currents through $M_{1,3}$ and $M_{2,4}$ rather than using it as a voltage multiplier. In this way, exponential currents can be eliminated at load as long as

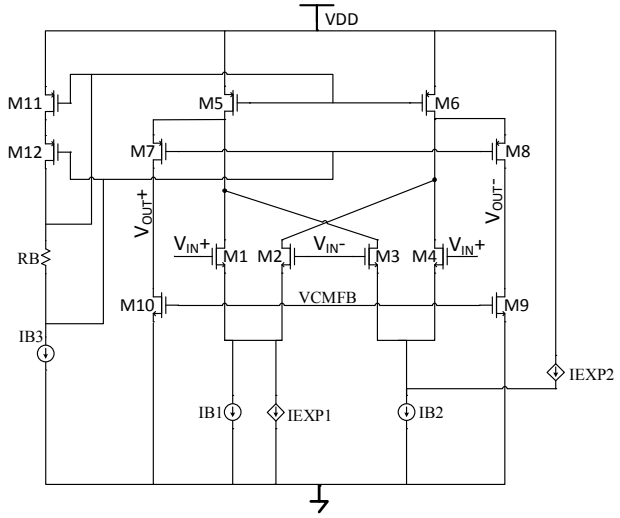

Fig. 1. The proposed VGA core

their effects to the tail currents are opposite. The circuit has a folded cascode structure to improve the input common-mode range, which is limited for the telescopic cascode structure. $M_{1,3}$ and $M_{2,4}$ are drain-coupled transistors with complementary inputs. I_{B1} and I_{B2} are independent current sources, whereas I_{EXP1} and I_{EXP2} are voltage-controlled current sources (controlled by V_{ctrl} as will be mentioned later), which provide gain variation. I_{B3}, R_B, M_{11} and M_{12} constitute a wide-swing cascode current source, providing bias currents for $M_{5,6}$ and $M_{7,8}$. An external common-mode feedback (CMFB) circuit sets the gate voltages of $M_{9,10}$ and common-mode output DC voltages. In Eqs. (1) and (2), the DC bias currents of $M_{1,2}$ and $M_{3,4}$ are given, respectively.

$$I_{D1,2} = \frac{I_{B1} + I_{EXP1}}{2} \tag{1}$$

$$I_{D3,4} = \frac{I_{B2} - I_{EXP2}}{2} \tag{2}$$

$M_{5,6}$ have a constant DC bias current with mirror action of M_{11}. On the other hand, $I_{D7,8,9,10}$ may vary greatly over the voltage gain range. In Eq. (3), the DC drain currents of those transistors are given:

$$I_{D7,8,9,10} = \frac{2I_{D5,6} - I_{B1} - I_{EXP1} - I_{B2} + I_{EXP2}}{2} \tag{3}$$

According to Eq. (3), I_{EXP1} must be equal to I_{EXP2} to keep the VGA's bandwidth independent of its voltage gain. When this condition is met, Eq. (3) yields to Eq. (4).

$$I_{D7,8,9,10} = \frac{2I_{D5,6} - I_{B1} - I_{B2}}{2} \tag{4}$$

Eq. (4) indicates that the VGA's load transistors have a constant DC bias current, which leads to a constant bandwidth over the gain range. Assuming that $I_{EXP1}=I_{EXP2}=I_{EXP}$, the transconductances of the input transistors are given by Eq. (5), where $\beta=0.5\mu_n C_{ox}W/L$.

$$g_{m1,2} = \sqrt{\beta(I_{B1} + I_{EXP})},\ g_{m3,4} = \sqrt{\beta(I_{B2} - I_{EXP})} \tag{5}$$

The gain of the VGA core is given in Eqn. (6), where R_{out} is the total output resistance.

$$K = 2(\sqrt{\beta(I_{B1} + I_{EXP})} - \sqrt{\beta(I_{B2} - I_{EXP})})R_{out} \tag{6}$$

If Eq. (6) provides the condition $I_{B1}=I_{B2}=I_B=I_{EXPmax}$, the corresponding maximum and minimum voltage gains can be expressed by Eq. (7), where I_{EXPmax} and I_{EXPmin} are the maximum and minimum currents, generated by the control voltage, respectively.

$$K_{\max} = \sqrt{8\beta I_{EXP\max}}R_{out},\quad K_{\min} = \sqrt{8\beta I_{EXP\min}{}^2 / I_B}R_{out} \tag{7}$$

Eq. (7) is valid, if $I_{EXPmax} \approx I_B$, then the voltage gain range provided by the exponential control block will be maintained by the VGA core. In Eq. (8), the currents flowing through $M_{1,2}$ and $M_{3,4}$ are given for both the lowest and highest gain conditions.

$$I_{D1,2}(K_{\min}) = \frac{I_B + I_{EXP\min}}{2} \cong \frac{I_B}{2} \tag{8a}$$

$$I_{D1,2}(K_{\max}) = \frac{I_B + I_{EXP\max}}{2} \cong I_B \tag{8b}$$

$$I_{D3,4}(K_{\min}) = \frac{I_B - I_{EXP\min}}{2} \cong \frac{I_B}{2} \tag{8c}$$

$$I_{D3,4}(K_{\max}) = \frac{I_B - I_{EXP\max}}{2} \cong 0 \tag{8d}$$

Mismatch effect creates an offset voltage at the output, which reduces the VGA's performance, especially for high gain conditions. Even worse, the VGA may saturate and become completely dysfunctional. Thus, a DC offset cancellation (DCOC) network must be used along with the VGA core, to reduce the offset automatically. In Fig. 2, the full VGA system is given. The details of the CMFB and DCOC circuits will not be discussed here. As shown in Fig. 2, V_{ctrl} is the control voltage that generates I_{EXP} to provide linear-in-dB gain for the VGA. The CMFB circuit detects and cancels the differential voltage at the output, with an error amplifier and closes the loop with $M_{9,10}$ shown in Fig. 1.

3. VGA Design Procedure

Noise figure (NF) and third-order input intercept point (IIP_3) are critical performance parameters for a VGA. Noise figure is

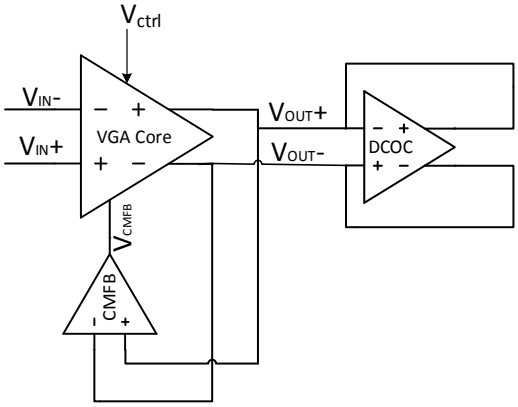

Fig. 2. The proposed VGA with DCOC and CMFB circuits

optimized at the highest gain where the input signal is lowest whereas IIP_3 is optimized at the lowest gain, where the input signal is highest.

The requirements of the VGA may change according to the receiver architecture. In Fig. 3, a generic WiMAX receiver architecture is given [7]. As an example, if the LNA has 2.5dB NF, -6dBm IIP3 and the mixer has 10dB NF, 9dBm IIP_3, then the VGA is optimized for 16dB NF and 12dBm IIP_3 [7].

IIP_3 predominantly depends on the overdrive voltages (V_{DSAT}) of the input transistors for a differential amplifier, as given in Eq. (9) [8].

$$IIP_{3\,RMS}\ (K_{\min}) = 3.3V_{DSAT} \tag{9}$$

Noise performance of the proposed VGA core mostly depends on $M_{1,2}$ and $M_{5,6}$. In Fig. 1, the noise originating from the tail currents (I_B and I_{EXP}) and $M_{7,8}$ (cascode transistors) can be neglected [9]. Assuming $M_{9,10}$ conduct much less current than $M_{1,2,5,6}$ and $M_{5,6}$ have the same V_{DSAT} as $M_{1,2}$, noise analysis for the VGA yields the input referred noise as given in Eq. (10), where k is the Boltzmann's constant and T is absolute temperature.

$$V_{inN}{}^2(K_{\max}) = \frac{32kT}{g_{m1,2}} \tag{10}$$

As the first step of the design procedure, Eq. (9) is used for choosing the V_{DSAT} values of the input transistors at the lowest gain. Then, Eq. (10) determines the currents flowing through $M_{1,2}$ at the highest gain. Combining Eqs. (8b), (9) and (10), results with I_B=5.7 mA and $(W/L)_{1,2,3,4}$=72. In order to increase the noise performance, $I_{D5,6}$ and $(W/L)_{5,6}$ are chosen as 6 mA and 330, respectively. In Table 1 and 2, all transistor sizes and other components' (current sources, resistors) values are given. The circuit is optimized for NF=10 dB (@27° C) and IIP_3=15 dBm to provide a safety margin.

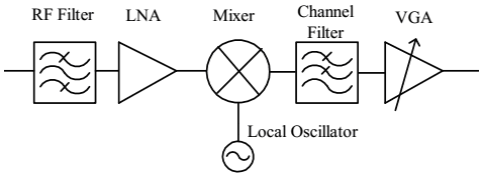

Fig. 3. WiMAX receiver [7]

Table 1. The size of transistors in the VGA core

Transistor	W (µm)	L (µm)
$M_{1,2,3,4}$	60	0.72
$M_{5,6}$	120	0.36
$M_{7,8}$	24	0.36
$M_{9,10,11}$	4	0.36
M_{12}	16	0.36

Table 2. Component values in the VGA core circuit

R_B	2 kΩ
I_{B3}	200 µA
$I_{B1}=I_{B2}=I_B$	5.7 mA
$I_{EXP1}=I_{EXP2}=I_{EXP}$	$f(V_{ctrl})$

4. Simulation Results

The proposed VGA circuit is shown in Fig. 1, was designed following the design procedure outlined in Section 3 using the TSMC 180 nm CMOS technology with 1.8 V single supply voltage and simulated using Cadence Analog Virtuoso. In Fig. 4, the variation of the VGA voltage gain as a function of the control voltage is given. The linear-in-dB gain range is approximately between -16 dB and 32 dB with 1.5 dB linearity error. The control voltage varies between -100 mV and 400 mV, which is dictated by the I_{EXP1} and I_{EXP2} function generators.

Fig. 5 shows the bandwidth variation, which should remain constant as the control voltage changes. The bandwidth is between 440 MHz and 450 MHz, corresponding to a 10 MHz variation, which is quite low.

In Fig. 6, the frequency response of the VGA voltage gain magnitude is plotted for different gain values. The low pass characteristic comes from parasitic, and load capacitances whereas the high pass characteristic comes from DCOC. The low corner frequency is approximately at 8 MHz, and the high corner frequency is approximately at 450 MHz. Fig. 6 also verifies an almost constant bandwidth for the VGA as the control voltage varies.

In Fig. 7, the NF is given for the highest gain. NF is smaller than 15 dB between 10 MHz and 450 MHz, the operating range of the VGA. Specifically, at 10 MHz and 450 MHz, the NF is 14.4 dB and 10.9 dB, respectively. As the frequency decreases, flicker noise starts to affect the noise performance, the NF increases.

In order to demonstrate the IIP_3 performance, harmonic balance simulation is performed with a two-tone test. The frequencies are selected as 100 MHz and 101 MHz. As can be seen in Fig. 8, IIP3 is equal to 14 dBm.

5. Conclusions

In this paper, a new VGA is proposed. The main advantage of the circuit is to provide constant bandwidth, independent of gain variation. The VGA is optimized for WiMAX (IEEE 812.16g) receivers. The simulations show that the proposed VGA core approximately consumes 21.6 mW power, has suitable noise and linearity performance for WiMAX receivers. Its bandwidth is high enough to provide flexibility when choosing the IF frequency. In Table 3, a summary of performance parameters is given. The simulations were performed with TSMC 180 nm technology and using Cadence Analog Virtuoso environment.

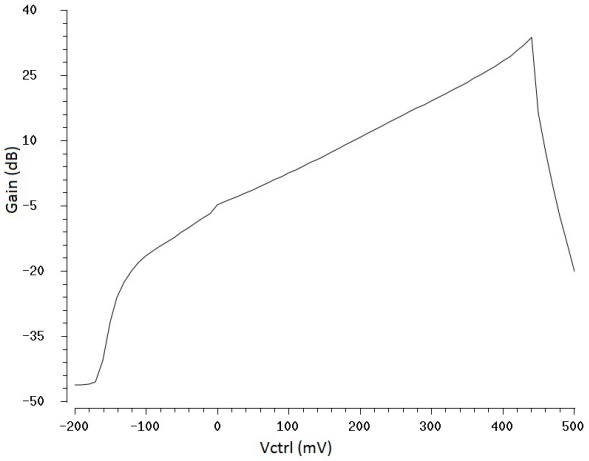

Fig. 4. VGA voltage gain as a function of the control voltage

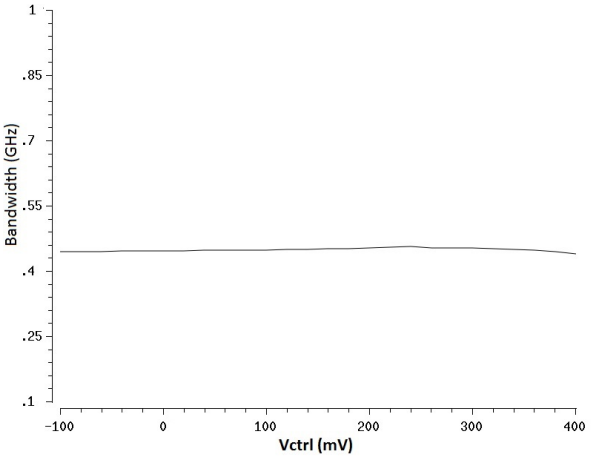

Fig. 5. VGA bandwidth as a function of the control voltage

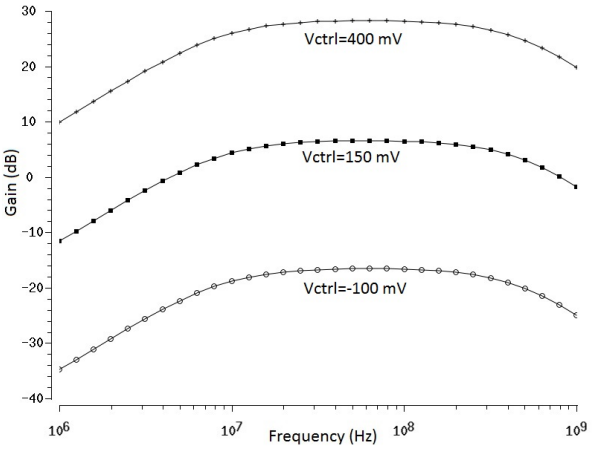

Fig. 6. Frequency response of the VGA voltage gain for different gain values

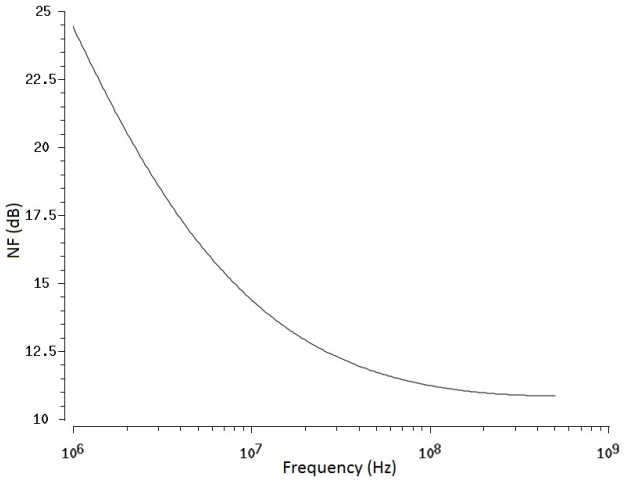

Fig. 7. NF of the VGA for maximum gain

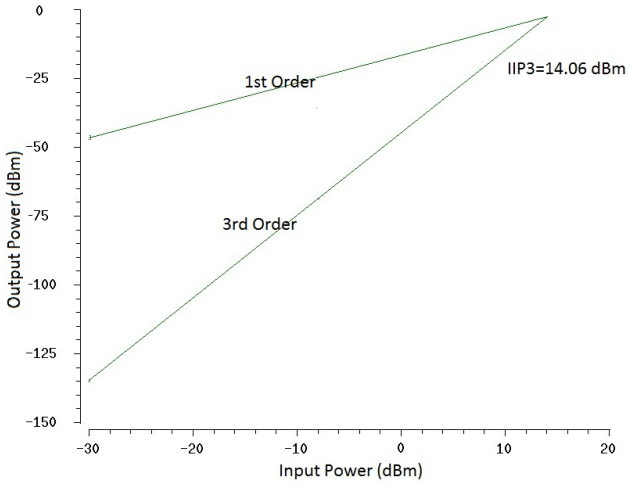

Fig. 8. IIP_3 of the VGA for minimum gain

Table 3. Performance summary of the VGA

Linear-in-dB gain variation	48 dB (-16 dB to 32 dB)
Bandwidth	450 MHz
NF @ max gain (100 MHz)	11.5 dB
IIP3 @ min gain (100 MHz)	14 dBm
DCOC frequency	≤ 10 MHz
Power consumption of the VGA core	21.6 mW

6. References

[1] Y. Chen, Y. Zheng, "A low-power variable-gain amplifier with improved linearity: Analysis and design", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Volume 59, Issue 10, pp. 2176-2185, February 2012.

[2] O. Jeon, R.M. Fox, B.A. Myers, "Analog AGC circuitry for a CMOS WLAN receiver", *IEEE Journal of Solid-State Circuits*, Volume 41, Issue 10, pp. 2291-2300, September 2006.

[3] F. Carrara, G. Palmisano. "High-dynamic-range VGA with temperature compensation and linear-in-dB gain control", *IEEE Journal of Solid-State Circuits*, Volume 41, Issue 10, pp. 2019-2024, September 2005.

[4] J.M. Khoury, "On the design of constant settling time AGC circuits", *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Volume 45, Issue 3, pp. 283-294, March 1998.

[5] Q.H. Duong, Q. Le, C.W. Kim, "A 95-dB linear low-power variable gain amplifier", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Volume 53, Issue 8, pp.1648-1657, August 2006.

[6] T. Arthansiri, V. Kasemsuwan, "Current mode pseudo exponential control variable gain amplifier using fourth-order Taylor's series approximation", *Electronics Letters*, Volume 42, Issue 7, pp. 379-380, March 2006.

[7] D. Ayadi, S. Rodriguez, "System level design of radio frequency receiver for IEEE 802.16 standard", *Design and Test Workshop: IDT 2008 3rd International*, Monastir, Tunisia, 2008, pp. 82-86.

[8] W.M.C Sansen, "Analog design essentials", Springer Science & Business Media, 2007.

[9] B. Razavi, "Design of analog CMOS integrated circuits", McGraw-Hill Education, 2001.