Fractional-Order Elements of Complement Order

Jaroslav Koton[1,2], Norbert Herencsar[1], David Kubanek[1], and Costas Psychalinos[3]

[1] Brno University of Technology, Technicka 12, 616 00 Brno, Czech Republic
{koton, herencsn, kubanek}@feec.vutbr.cz
[2] RUDN University, 6 Miklukho-Maklaya st, Moscow, 117198, Russian Federation
[3] Physics Department, Electronics Laboratory, University of Patras, Rio Patras, Greece,
cpsychal@upatras.gr

Abstract

The design of analogue fractional-order systems requires the presence of fractional-order elements (FOEs), capacitive and/or inductive, featuring fractional order α ($0 < \alpha < 1$). As currently FOEs are not available as discrete elements, suitable RC networks are used to overcome this obstacle. In this paper we primary propose the transformation of fractional-order elements to cover the whole span of α by a reduced number of RC networks or later readily available discrete FOEs. Using this approach, FOEs can be designed featuring complementary fractional order β, i.e. $\beta = 1 - \alpha$. Analysing the transformation possibilities, we also discuss the design of fractional capacitance multiplier.

1. Introduction

Fractional-order calculus gains significant attention in the last decades as it can be applied in various research areas, e.g. chemistry, medicine, thermodynamics, control etc. [1], [2]. From the area of electrical engineering, the signal processing and generation are the main domains, where even basic fractional-order filters and oscillators offer new benefits with regards to their integer-order (classic) counterparts [3].

Assuming "classic" linear analogue function blocks, the resistors, capacitors and inductors generally represent the main discrete elements used for the design. Once designing fractional-order systems, the capacitive and inductive fractional-order elements (FOEs), also called Constant Phase Elements (CPEs) or Elements with Fractional Impedance (EFIs) are required. Similarly as in classic circuit design the capacitors are preferred to inductors, the main attention is paid to capacitive FOEs featuring fractional order α ($0 < \alpha < 1$) and pseudo-capacitance C_α. The first attempts of direct implementation of capacitive FOEs as discrete elements can be found in the literature. These discrete FOEs are based on various design approaches and materials, such as poly-vinylidene fluoride [4], ionic polymer metal composites [5], polymer-carbon nanotubes [6], structures with distributed parameters [7] etc., however still are not readily available and the fractional feature is valid in a limited frequency range. Therefore, to approximately emulate capacitive FOE, a suitable RC network is designed, whereas an overview of possible structures can be found in [8]. Although, there are techniques to determine the values of the resistors and capacitors in such networks, according to the required accuracy of the approximation, relatively high number of resistors and capacitors with high ratio (even three decades [8]) in values is required. Once adjustability of function blocks' parameters should also be present, it is required to switch between several RC networks, or between discrete FOEs in the future, as any change in parameters requires another FOE with different order α and/or pseudo-capacitance C_α.

With the aim to reduce the number of required RC networks, and even discrete FOEs in the future designs, we discuss the transformation technique to obtain mainly complementary fractional orders. Based on that, the number of the required RC networks (or FOEs) can be halved. Furthermore as it will be shown, not only the complementary fractional orders can be achieved through the transformation, but also capacitive FOEs with adjusted pseudo-capacitances.

2. Fractional-order elements

The fractional-order element (FOE), most commonly understood as fractional-order (or fractional) capacitor C_α, is described by its impedance:

$$Z_{C\alpha} = \frac{1}{\omega^\alpha \cdot C_\alpha} \exp\left(-j\alpha\frac{\pi}{2}\right), \tag{1}$$

whereas $0 < \alpha < 1$ is the fractional order and C_α, expressed in [F/s$^{1-\alpha}$], is the pseudo-capacitance, respectively. According to (1), the phase shift between the cross voltage and through current of a fractional capacitor is $-\alpha\frac{\pi}{2}$ and is constant in the whole frequency range.

At a specific frequency ω_0, using [8] an equivalent capacitance C (in Farads) featuring the same impedance as a fractional capacitor can be determined:

$$C = \frac{C_\alpha}{\omega_0^{1-\alpha}}, \tag{2}$$

whereas ω_0 mostly defines the central frequency of the frequency range, where the fractional feature of the FOE (i.e. the phase is understood to be constant) is present.

This work was supported by Czech Science Foundation under grant no. 16-06175S and the National Sustainability Program under grant LO1401. For the research, infrastructure of the SIX Center was used. The publication was supported by the Ministry of Education and Science of the Russian Federation the Agreement number No. 02.a03.21.0008. This article is based upon work from COST Action CA15225, a network supported by COST (European Cooperation in Science and Technology).

3. Transformation of FOEs

A significant area of classic analogue circuit design is devoted to the design of synthetic inductors or also referred to as inductor simulators as they enable to omit the discrete inductors in the circuit design. For this sake, the gyrators are used that generally transform the capacitive load to a lossy or loss-less inductance. A variety of such impedance converters can be found in the open literature, where the authors use different types of active elements to design grounded or floating lossy or loss-less inductance simulators [9]-[12]. Based on the this approach, not only synthetic inductors but also e.g. the frequency dependent negative resistors (FDNRs) are described and used in analogue circuit design [12]-[14].

The idea of converting the impedance can also be advantageously applied to the area of fractional-order elements. Let us assume a general impedance converter as shown in Fig. 3 that contains three admittances Y_1, Y_2 and Y_3 as passive elements and a network of generally arbitrary types of active elements. Let the input impedance Z_{IN} of this general impedance converter be determined as:

$$Z_{IN} = \frac{Y_1}{Y_2 Y_3}. \tag{3}$$

Selecting the specific type (i.e. resistor, capacitor and/or capacitive fractional-order element with the fractional order α) of the individual admittances Y_1, Y_2 and Y_3, the capacitive FOE with complementary order can be designed if $Y_1 = s^{\alpha}C_{\alpha}$, $Y_2 = sC$, $Y_3 = G$, since the input impedance of the impedance converter will be described as:

$$Z_{IN}(s) = \frac{1}{s^{\beta}C_{\beta}}, \tag{4}$$

where $\beta = 1 - \alpha$ is the fractional order of the new capacitive FOE with its pseudo-capacitance $C_{\beta} = (CG)/C_{\alpha}$.

The fact of obtaining FOEs with fractional order being complementary (i.e. β) to the original fractional order (i.e. α) of the assumed capacitive FOE may result in a significant reduction of discrete FOEs being required for the design, mainly in case of implementing the fractional function blocks as integrated circuits that should offer sufficient tunability and adjustability.

Selecting $Y_1 = G_1$, $Y_2 = s^{\alpha}C_{\alpha}$, $Y_3 = G_3$, the impedance converter can be also used as fractional capacitor multiplier as the input impedance is:

$$Z_{IN}(s) = \frac{1}{s^{\alpha}C_{\alpha}} \cdot k, \tag{5}$$

where $k = G_1/G_3$ is the pseudo-capacitance multiplier and it can be evident that the fractional order α remains unchanged.

From (4) and (5) it is clear that the required fractional order and/or the value of the pseudo-capacitance can be adjusted by properly selecting the parameters of the passive elements. Also notice that in case of impedance converter being used to obtain a fractional-order element with complementary fractional order and also in the case of pseudo-capacitance multiplier the general admittance Y_3 has the character of a conductor. Hence, for the design of the impedance converter the operational transconductance amplifier (OTA) defined with its adjustable transconductance g_m can be advantageously used as it offers the possibility of electronic adjustablity of the pseudo-capacitance of the final fractional-order element.

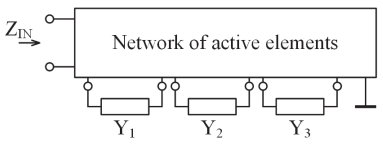


Figure 1. General view on impedance converter.

4. Implementation example

To verify the theory of impedance conversion of fractional-order elements, we analyse the performance of the impedance converter as described below. For the implementation, one current conveyor and one operational transcoductance amplifier as active elements are used.

4.1. Active elements

The current conveyors represent a wide group of active elements, where an comprehensive overview can be found e.g. in [15]. For our purpose we use probably the most frequently discussed type, the second generation current conveyor CCII (Fig. 2(a)), whose behaviour is defined by the following set of equations:

$$v_X = v_Y, \;\; i_Y = 0, \;\; i_Z = i_X. \tag{6}$$

To follow the idea of enabling also the electronic controllability as described in the section above, the operational transcoductance amplifier (OTA) is advantageously used in the design of the impedance converter as the second active element with the behaviour simply described as:

$$i_{OUT} = g_m(v_+ - v_-), \tag{7}$$

where the transconductance g_m can be most commonly adjusted by an external dc current I_{SET} as shown in Fig. 2(b).

4.2. General impedance converter

Using the selected types of active elements, the impedance converter still using general admittances Y_1 and Y_2 is shown in Fig. 3. The input impedance of this circuit can be determined as:

$$Z_{IN} = \frac{Y_1}{Y_2 \cdot g_m}, \tag{8}$$

and hence from the formal point of view fully corresponds to (3), where $Y_3 = g_m$. Selecting the type of the admittances Y_1 and Y_2 according to the cases as described in the section above, the grounded fractional capacitor with the order α or β ($\beta = 1-\alpha$) and adjustable pseudo-capacinace can be designed, see Fig. 4, where the final impedance converter solutions with specific types of passive elements are shown.

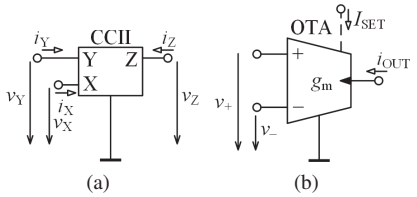


Figure 2. Schematic symbol of (a) second generation current conveyor (CCII) and (b) operational transconductance amplifier (OTA)

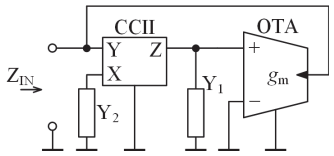


Figure 3. General impedance converter using CCII and OTA

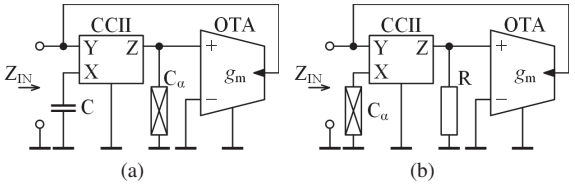


Figure 4. Final solution of the impedance converter (a) to obtain FOE with complementary fractional order β (b) operating as pseudo-capacitance multiplier.

5. Performance analysis and simulations

The transformation of FOEs within the cases discussed in Section 3 is analysed. For this purpose, using the approach described in [8] the RC network approximating the capacitive FOE with fractional order $\alpha = 0.2$, and at central frequency $f_0 = 1$ kHz featuring equivalent capacitance 1 nF, i.e. having pseudo-capacitance $C_\alpha = 1.1\ \mu\text{Fs}^{-0.8}$, is used and designed according to Cauer I topology as shown in Fig. 5. The values of the passive elements in this RC network are as follows: $R_0 = 100.3\ \text{k}\Omega$, $R_1 = 63.4\ \text{k}\Omega$, $R_2 = 59.2\ \text{k}\Omega$, $R_3 = 55.8\ \text{k}\Omega$, $R_4 = 56.7\ \text{k}\Omega$, $R_5 = 63.9\ \text{k}\Omega$, $C_1 = 200.7$ pF, $C_2 = 1.3$ nF, $C_3 = 3.8$ nF, $C_4 = 9.2$ nF, and $C_5 = 23.9$ nF [8]. Note that the ratio between the maximum and minimum vales of resistors is 1.79, while for capacitors the corresponding value is 119.

The module and phase response of input impedance of the FOE using the Cauer I topology is shown in Fig. 6. As the assumed fractional order of the FOE is $\alpha = 0.2$, the FOE is expected to have the constant phase of -18 deg. This presumption is proved by the phase response as shown in Fig. 6(b).

To design a FOE with the fractional order 0.8 featuring an equivalent capacitance of 1 nF at $f_0 = 1$ kHz, the RC network from Fig. 5 can be used again. However, according to [8] the values of the resistors R_0 and R_5 from the Cauer I RC network are from the range of MΩ and furthermore, the ratio between the maximum and minimum value of resistors is 3887, which can be seen as disadvantageous.

Using the impedance converter, the original FOE from Fig. 5 featuring $\alpha = 0.2$ and equivalent capacitance of 1 nF at $f_0 = 1$ kHz, i.e. $|Z| = 159.2\ \text{k}\Omega$ and $C_\alpha = 1.1\ \mu\text{Fs}^{-0.8}$ can be easily transformed. Using (2), for $\beta = 1 - \alpha = 0.8$ and equivalent capacitance of 1 nF at $f_0 = 1$ kHz the pseudo-capacitance C_β can be determined to be $5.75\ \text{nFs}^{-0.2}$. Assuming the final circuit of the impedance converter as shown in Fig. 4(a), using the original FOE with fractional order $\alpha = 0.2$, and setting $C = 200$ pF and $G = g_m = 31.6\ \mu$S a grounded fractional capacitor featuring fractional order $\beta = 0.8$ and pseudo-capacitance $C_\beta = 5.75\ \text{nFs}^{-0.2}$ is obtained. In Fig. 7, the module and phase response obtained using the OrCAD PSpice simulator are shown, whereas the active elements were emulated using UCC-N1B integrated circuit [16]. Changing the transconductance g_m the pseudo-capacitance C_β of the fractional capacitor can be adjusted without affecting the fractional-order β as it can be seen from Fig. 7. For the selected values of $g_m = \{15.7,\ 31.6,\ 63.3\}\ \mu$S, the value of the pseudo-capacitance C_β is $\{2.88,\ 5.75,\ 11.5\}\ \text{nFs}^{-0.2}$, which according to (2) corresponds to equivalent capacitance of $\{0.5,\ 1,\ 2\}$ nF at frequency $f_0 = 1$ kHz. The ratio between the maximum and minimum values of resistors and capacitors remains the same as it is in case of the original FOE.

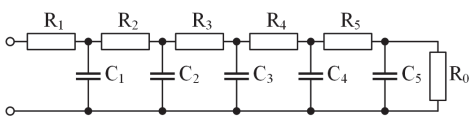


Figure 5. RC network for FOE emulation using Cauer I topology [8].

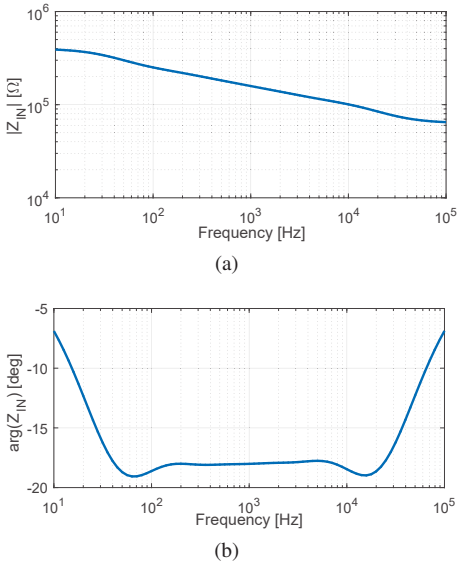
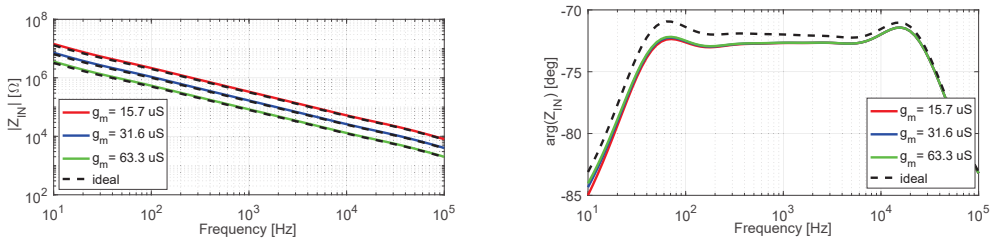


Figure 6. (a) Module and (b) phase response of the "original" FOE from Fig. 5 for $\alpha = 0.2$, $C_\alpha = 1.1\ \mu\text{Fs}^{-0.8}$.

The performance of the impedance converter from Fig. 4(b) that operates as pseudo-capacitance multiplier has been also analysed. Using the original FOE from Fig. 5 with fractional order $\alpha = 0.2$ and selecting $R = 31.6\ \text{k}\Omega$ ($G = 31.6\ \mu$S), for $g_m = \{15.7,\ 31.6,\ 63.3\}\ \mu$S the multiplication factor k is $\{2,\ 1,\ 0.5\}$ and the final (transformed) pseudo-capacitance $C_{\alpha T}$ will be $\{0.55,\ 1.1,\ 2.2\}\ \mu\text{Fs}^{-0.8}$. Using (2) the equivalent capacitance of transformed fractional capacitor is again $\{0.5,\ 1,\ 2\}$ nF. The input impedance module and phase responses for the selected values of g_m are shown in Fig. 8. From Fig. 8(a) it can be seen that changing g_m also the module changes, whereas the phase (Fig. 8(b)) is nearly constant as the phase shift of the original FOE with $\alpha = 0.2$ in the same frequency range.

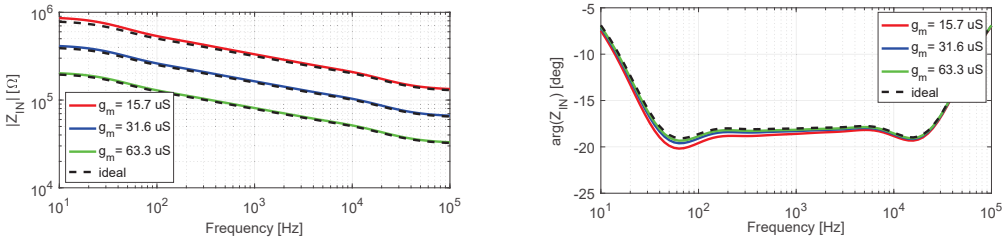
6. Conclusion

In the paper we proposed the utilization of general impedance converters primarily for the design of capacitive FOEs with fractional order being complementary to the original FOE with the aim to reduce the number of FOEs being required



(a) (b)

Figure 7. (a) Module and (b) phase response of the FOE with complementary fractional order $\beta = 1 - \alpha = 0.8$.



(a) (b)

Figure 8. (a) Module and (b) phase response of the impedance converter operating as pseudo-capacitance multiplier of a FOE with $\alpha = 0.2$.

in future circuit designs. Using a simple impedance converter employing single second generation current conveyor and single operational transcoductance amplifier, we have shown efficient transformation of a capacitive FOE with fractional order of 0.2 to a capacitive FOE with fractional order of 0.8. Furthermore, the usage of OTA in the impedance converter presents the possibility of adjusting the pseudo-capacitance of the fractional capacitor.

7. References

[1] T. J. Freeborn, "A survey of fractional-order circuits models for biology and biomedicine", *IEEE Trans. Emerg. Sel. Topics Circuits Syst.*, vol. 3, no. 3, pp. 416-424, 2013.

[2] M. D. Ortigueira, "An introduction to the fractional continuous time linear systems: The 21st century systems", *IEEE Circuits Syst. Mag.*, vol. 8, no. 3, pp. 16-26, 2008.

[3] A. Elwakil, "Fractional-order circuits and systems: an emerging interdisciplinary research area", *IEEE Circuits Syst. Mag.*, vol. 10, no. 4, pp. 40-50, 2010.

[4] A. Agambayev, S. P. Patole, M. Farhat, A. Elwakil, H. Bagci, and K. N. Salama, "Ferroelectric Fractional-Order Capacitors", *ChemElectroChem*, 2017, doi: 10.1002/celc.201700663.

[5] M. Shahinpoor, "Ionic Polymer Metal Composites (IPMCs), Smart Multi-Functional Materials and Artificial Muscles, Vol. 2", *The Royal Society of Chemistry*, 2016, ISBN: 978-1-78262-721-0.

[6] D. A. John, S. Banerjee, G. W. Bohannan, and K. Biswas, "Solid-state fractional capacitor using MWCNT-epoxy nanocomposite", *Applied Physics Letters*, vol. 110, no. 16, ID 163504, 2017.

[7] A. Kh. Gil'mutdinov, P.A. Ushakov, and E. Khazali, "Fractal Elements and their Applications", *Springer*, 2017, ISBN: 978-3-319-45248-7.

[8] G. Tsirimokou, "A systematic procedure for deriving RC networks of fractional-order elements emulators using MATLAB", *AEU - Int. J. Electronics and Communications*, vol. 78, pp. 7-14, 2017.

[9] D. F. Berndt and S. C. Dutta Roy, "Inductor simulator using a single unity gain amplifier", *IEEE J. Solid-State Circuits*, vol. 4, no. 3, pp. 161-162, 1969.

[10] A. Antoniou, "Realisation of gyrators using operational amplifiers, and their use in RC-active-network synthesis", *IEE Proc.*, vol. 116, no. 11, pp. 1838-1850, 1969.

[11] F. Kacar and H. Kuntman, "CFOA-based lossless and lossy inductance simulators", *Radioengineering*, vol. 20, no. 3, pp. 627-631, 2011.

[12] J. Koton, N. Herencsar, and M. Venclovsky, "History, progress and new results in synthetic passive element design employing CFTAs", *Int. J. Adv. Telecommun. Electron. Sig. Systs.*, vol. 4, no. 1, pp. 15-26, 2015.

[13] G. C. Temes and J.W. Lapatra, "Introduction to Circuit Synthesis and Design", chapter 6, *McGraw-Hill*, 1977.

[14] W.-S. Chung, H.-J. Kim, and K.-M. Cho, "Current-controllable FDNRs using linear transcapacitance amplifiers", *Int. J. Electronics*, vol 91, no. 7, pp. 421-430, 2004.

[15] R. Senani, D. R. Bhaskar, and A. K. Singh, "Current conveyors: variants, applications and hardware implementations", *Springer*, 2015.

[16] Datasheet UCC-N1B: Universal Current Conveyor (UCC) and Second-Generation Current Conveyor (CCII+/-), Brno University of Technology, 2010, Rev.0, www.utko.feec.vutbr.cz/koton/soubory/UCC_N1B_Rev0.pdf.