Evaluation of Zero Voltage Switching SEPIC Converter for Module Integrated Distributed Maximum Power Point Tracking Applications

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Abstract

In this paper, the quasi-resonant SEPIC converter topology is evaluated for module integrated distributed maximum power point trackers (DMPPTs) which may increase energy capture from the photovoltaic modules operating with non-uniform irradiation conditions. Operating principals of the proposed module integrated converter is analyzed in steady-state condition and verified by simulation. The maximum converter efficiency is obtained as 94.7%. The advantages, difficulties and zero voltage switching regions of proposed converter are also presented. In addition, DMPPT performance of the proposed converter is evaluated via simulations and the results are presented.

1. Introduction

In recent decades, photovoltaic electricity has become one of the most studied subjects with developments in power electronics and solar cell technologies. In conventional maximum power point tracking(CMPPT) grid connected PV system architecture, PV panels are connected in series to obtain a PV string which has high dc voltage close to the utility grid. The PV strings may be connected in parallel to increase the power, and then it is connected to the grid through a central inverter. However, the string arrangement is vulnerable to shading effects, and the generated power may greatly be reduced even when the part of PV modules is shaded by external factors such as clouds, buildings, trees etc.

In DMPPT architecture, each PV module has a dedicated dc-dc converter which performs an MPPT operation independent from other PV modules. Output terminals of these converters can be connected in series like as standard PV modules, and then attached to the input terminal of inverter. DMPPT topology can mitigate the negative effects caused by partial shading or any other mismatching conditions, by keeping each PV module at its own maximum power point.

In literature, many DMPPT architectures including dc-dc converter and dc-ac micro inverters have been proposed [1, 9]. Some of them include module-level dc-ac micro inverters [6, 9]. The micro inverter architecture may increase energy capture, but it requires high voltage gain from module voltage (e.g.20-40 Vdc) to grid voltage (e.g. 120-240 Vac rms). Thus, the micro inverters have lower efficiency than conventional high voltage inverters. Some studies prefer buck or boost type dc-dc converters [1, 6]. However, these converters have a disadvantage because they are not able to generate output voltages both above and below of the input voltage. In addition, some applications requires communication between central (or string) inverter and module integrated converter [9]. However, buck-boost converter and Cuk converter have advantage of voltage transformation but these converters may not achieve the same efficiency as the buck or boost converters. All of these converters are subject to both conduction and switching losses.

In this paper, quasi-resonant (QR), zero voltage switching (ZVS) SEPIC converter topology is proposed for DMPPT as shown in Figure 1. The converter was analysed for a switching period in steady-state. The advantages, difficulties and simulation of proposed converter are examined. In addition, the performance of the proposed converter in DMPPT architecture is evaluated by simulation, and the results are presented.

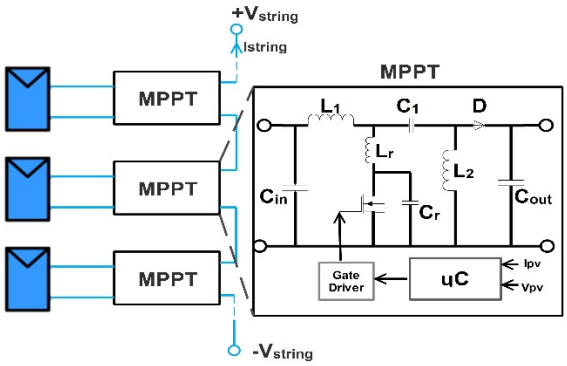

Fig. 1. DMPPT System Architecture

2. Analysis of Quasi-Resonant SEPIC Converter

Conventional PWM converters are operated under hard-switching conditions where the voltage and current of a switch changes at turn on and turn off which cause serious switching losses, switching stresses and electromagnetic interference. It also limits the maximum switching frequency because of switching losses are proportional to the switching frequency. If the overlapping of voltage and current waveforms of semiconductor devices are reduced, switching losses are minimized. Switching moments of semiconductor devices can be softened by adding resonant circuits in hard switching pulse width modulated (PWM) converters [10]. Because of lower values of resonant elements, soft switching is possible for high switching frequencies. Therefore, size and weight of converters are reduced. Over the past decades, numerous soft switching techniques have been proposed [11, 13]. This paper presents a quasi-resonant zero voltage switching SEPIC converter as shown in Figure 2. In ZVS topologies, the transistor turns on at zero voltage; therefore it reduces turn on switching losses to nearly zero. In QR ZVS converters, transistor output capacitance is merged with the resonant capacitance and similarly the diode lead inductance is merged with the resonant inductor. However, diode junction capacitance is not merged.

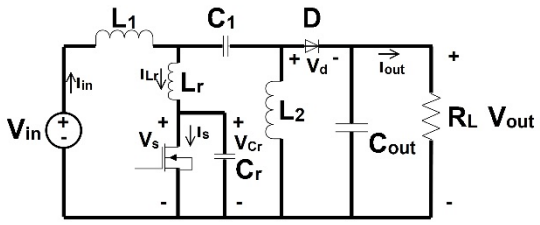

Fig. 2. Quasi-Resonant ZVS SEPIC Converter

In the analysis, the converter elements are accepted quite large with respect to the resonant elements and all of them are assumed as ideal. The resonant frequency and characteristic impedance of tank circuit are

$$\omega_o = \frac{1}{\sqrt{L_r C_r}} \tag{1}$$

$$Z_O = \sqrt{\frac{L_r}{C_r}} = \omega_o L_r = \frac{1}{\omega_o C_r} \tag{2}$$

The normalized load resistance is defined as

$$Q = \frac{R_L}{Z_O} = \frac{AR_L}{\omega_s L_r} = \frac{\omega_s C_r R_L}{A} \tag{3}$$

where $A=f_s/f_o$ is the normalized switching frequency. The normalized initial resonant inductor and switch currents when the switch turns on are can be defined as

$$h = \frac{i_{L_r}(0)}{I_{in} + I_{out}} = \frac{i_s(0)}{I_{in} + I_{out}} \tag{4}$$

The operation of QR ZVS SEPIC converter consists of four modes during the switching cycle as shown in Figure 3.

Mode 1 (0<t<t_1)

In this mode, switch and diode are both on. During this mode, current of switch is;

$$i_s = \frac{(I_{in} + I_{out})Q\omega_s t}{AM} + i_s(0) \tag{5}$$

where $M=V_{out}/V_{in}$ is the voltage transfer ratio. Similarly, current of diode is;

$$i_d = I_{in} + I_{out} - \frac{(I_{in} + I_{out})Q\omega_s t}{AM} - i_s(0) \tag{6}$$

This mode ends at "t_1" when the diode current reaches zero.

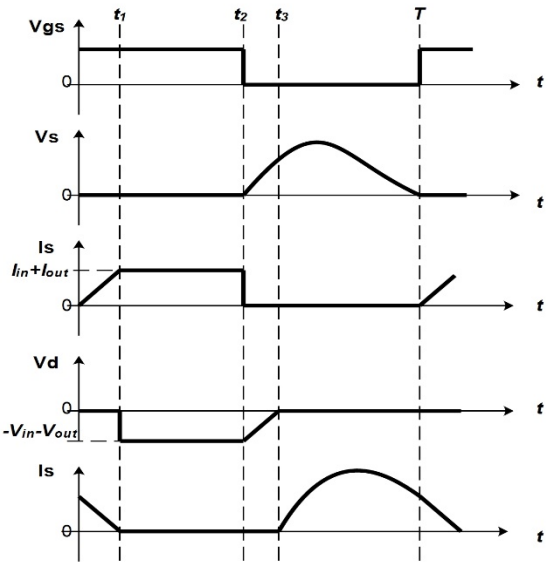

Fig. 3. Waveforms of QR ZVS SEPIC Converter

Mode 2 (t_1<t<t_2)

In this mode, the switch is on and diode is off. During this mode, current of switch is;

$$i_s = I_{in} + I_{out} \tag{7}$$

Similarly, voltage of diode is;

$$v_d = -V_{in} - V_{out} \tag{8}$$

This mode ends at "t_2" when the transistor is turned off by the gate driver.

Mode 3 (t_2<t<t_3)

In this mode, switch and diode are both off. During this mode, voltage of switch is;

$$v_s = \frac{M(V_{in} + V_{out})}{AQ}(\omega_s t - 2\pi d) \tag{9}$$

where d is duty cycle .Similarly, voltage of diode is;

$$v_d = (V_{in} + V_{out})\left(\frac{M}{AQ}(\omega_s t - 2\pi d) - 1\right) \tag{10}$$

This mode ends at "t_3" when the diode voltage reaches zero.

Mode 4 (t_3<t<T)

In this mode, Switch is off and diode is on. During this mode, voltage of switch is;

$$v_s = (V_{in} + V_{out})\left(1 + \frac{M}{Q}\sin\left(\frac{\omega_s t - \omega_s t_3}{A}\right)\right) \quad (11)$$

Similarly, current of diode is;

$$i_d = (I_{in} + I_{out})\left(1 - \cos\left(\frac{\omega_s t - \omega_s t_3}{A}\right)\right) \quad (12)$$

current in the resonant inductor can be found as;

$$i_{L_r} = (I_{in} + I_{out})\cos\left(\frac{\omega_s t - \omega_s t_3}{A}\right) \quad (13)$$

This mode ends at "*T*" when the transistor is turned on by the gate driver.

For ZVS operation, the following two equations should be satisfied;

$$v_s(T) = v_s(0) = 0 \quad (14)$$

$$i_{L_r}(T) = i_{L_r}(0) = h(I_{in} + I_{out}) = 0 \quad (15)$$

Using Eq.13, it can be written that

$$\frac{Q}{M} = -\sin\left(\frac{2\pi(1-d)}{A} - \frac{Q}{M}\right) \quad (16)$$

Normalized initial switch current is determined using Eq.4, Eq.5 and Eq.13.

$$h = \cos\left(\frac{2\pi(1-d)}{A} - \frac{Q}{M}\right) \quad (17)$$

Duty cycle is determined using Eq.16.

$$d = 1 - \frac{1}{2\pi}\left(\frac{f_s}{f_o}\right)\left(-\cos^{-1}\left(\sqrt{1-\left(\frac{Q}{M}\right)^2}\right) + \frac{Q}{M} + 2\pi n\right) \quad (18)$$

By assuming, *h=0* and *n=1*, the duty cycle can be approximated as;

$$d = 1 - \frac{3\pi + 2}{4\pi}\left(\frac{f_s}{f_o}\right) \cong 1 - 0.909\left(\frac{f_s}{f_o}\right) \quad (19)$$

It is seen that, the switching period has constant off time and variable on time. For ZVS operation, it should be obtained that

$$-1 \le h \le 1 \quad \text{or} \quad 0 \le Q = \frac{R_L}{Z_O} \le M \quad (20)$$

3. Converter Simulation Results

An example design is simulated with MATLAB-Simulink as shown in Fig.4. QR ZVS SEPIC converter elements are selected for 80W solar module so as to be the converter operates in continuous conduction mode at minimum switching frequency.

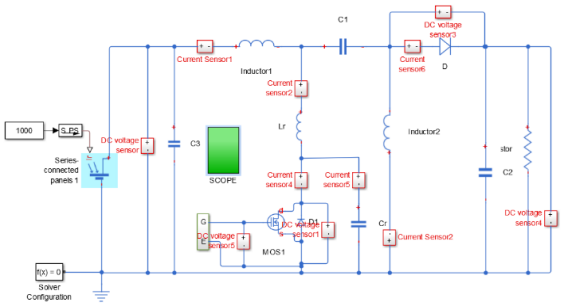

Fig. 4. Simulation Model of QR ZVS SEPIC Converter

Table-1 shows that values of both quasi-resonant SEPIC converter elements and their parasitic. The current and voltage waveforms of semiconductor devices are shown in Fig.5 for 1000W/m^2 solar radiation. It can be seen from the figure that the transistor turns on and off at zero voltage. Thus, stresses and losses caused by switching moments such as switching losses, switching stresses and EMI levels in converter can be reduced. However, converter does not merge with all parasitic components. The diode output capacitance and resonant inductor become a tank circuit when diode is off and causes power loss. Moreover, the transistor peak voltage for soft switching condition is higher than the hard switching which causes higher conduction loss of transistor.

The simulation results for 4 different solar radiations are shown in Table-2. It is obtained that the maximum converter efficiency is 94.7%. In addition, module output power is inversely proportional to the switching frequency.

For ZVS operation, normalized load resistance should be less than the voltage transfer ratio as it is mentioned in Eq.28. The converter has some difficulties at light load conditions. Fig.6 shows that ZVS operating region of converter with module characteristic for different load resistance values. The operating region was bounded to minimum and maximum values of MPPT module reference voltage in the x-axis (12-20V). When the load resistance value increased, the ZVS operating region has a more narrow area. Therefore, the string voltage and current values have influence upon ZVS operation in DMPPT architecture.

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Table 1. Converter Parameters Used in Simulation

	Value	Features
L1(Input Inductor)	150µH	R_S=0.01Ω
L2(Output Inductor)	150µH	R_S=0.01Ω
C1(Coupled Capacitor)	100µF	R_S=1µΩ
C2(Output Capacitor)	500µF	R_S=1µΩ
RL(Output Load)	5Ω	
Mosfet		R_{DS}=0.01Ω, C_{OSS}=150pF
Diode		V_F=0.52V, C_J=350pF
Lr(Resonant Inductor)	10µH	R_S=0.005Ω
Cr(Resonant Capacitor)	220nF	
fo(Resonant Frequency)	98kHz	

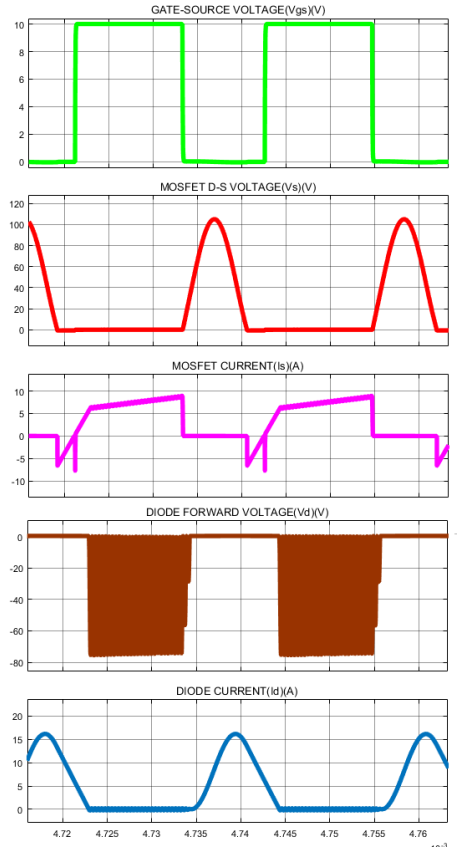

Fig. 5. Waveforms of Semiconductor Devices of Converter

Table 2. The Converter Simulation Results

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G(W/m^2)	f_s(kHz)	R_L(Ω)	Power$_{in}$(W)	Power$_{out}$(W)	μ(%)
1000	46.75	5	80.04	75.80	94.7
750	49.95	5	62.09	58.19	93.7
500	54.78	5	42.04	37.27	88.7
250	72.43	2	23.98	21.24	88.5

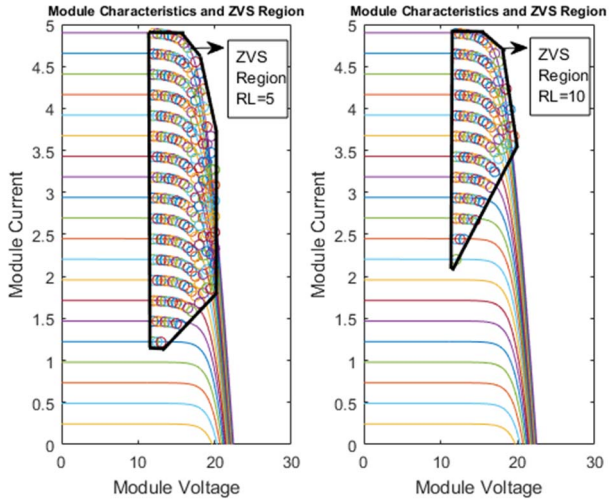

Fig. 6. ZVS Operating Region of Converter

4. DMPPT Architecture Simulation Results

A DMPPT architecture comprised of three 80W solar modules is simulated via in MATLAB-Simulink environment as shown in Fig.7. Inputs of modules are module solar radiation and module temperature. In simulation, each module has a dedicated dc-dc converter and output terminals of these converters connected is series to create a string and then it is connected to the input terminal of string regulator. In addition, each module has a MPPT algorithm and PI controller. The MPPT block consists of a perturbation and observation algorithm. The inputs of MPPT algorithm are the module voltage and current. The output of MPPT algorithm is the reference voltage for the module maximum power point. The PI controller ensures that the module voltage is equal to the desired reference value.

The solar radiation of module #3 is changed from 1000 W/m^2 to 500 W/m^2 at t=10s in simulation time. The solar radiation of

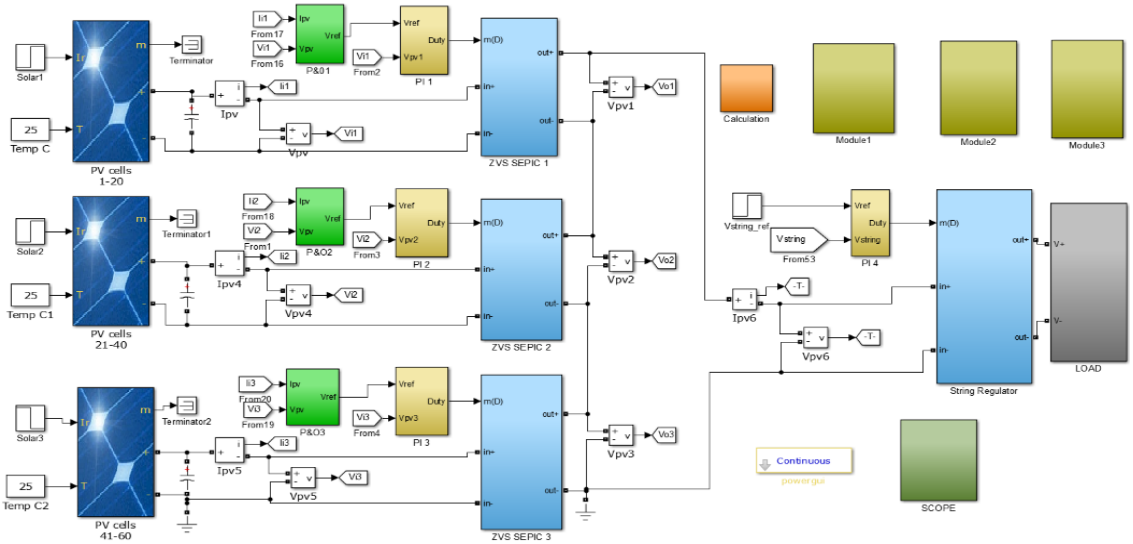

Fig. 7. DMPPT System Architecture Simulation Model

other modules are 1000 W/m^2 and constant. The string voltage, current and power waveforms are obtained for this condition as shown in Fig.8. As seen from the figure that the string voltage in steady state is kept at the desired reference value (60V).

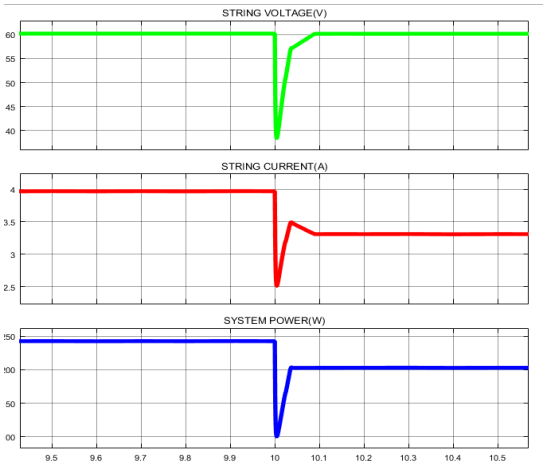

Fig. 8. String Waveforms

The different shading scenarios are also verified for both of the DMPPT and CMPPT by simulation and the results are summarized in Table-3. The simulation results show that when the solar radiation of all modules reduced equally, output load resistance of converter is increased because of constant string voltage. In addition, if the desired string voltage is high enough, when the converters are operated in high voltage gain, ZVS operation may not be implemented. When solar radiation of some of modules reduced, output load resistances of these modules reduce and these modules' converters have large ZVS operation area. However, the output load resistances of unshaded modules increase so the converters are more flexible for shaded modules. Moreover, the DMPPT architecture allows much more energy capture (E.C. in Table-3) than the CMPPT in non-uniform radiations. However, the CMPPT architecture is more advantageous for uniform radiations because of converter losses in the DMPPT architecture.

Table 3. The DMPPT Simulation Results

		DMPPT				CMPPT				
	G (W/m^2)	V_{out} (V)	I_{out} (A)	V_{string} (V)	P_{string} (W)	V_{out} (V)	I_{out} (A)	V_{string} (V)	P_{string} (W)	E.C. (%)
#1	1000	20.05				17.97				
#2	1000	20.05	3.96	60.15	238	17.97	4.48	53.91	241	-1,2
#3	1000	20.05				17.97				
#1	1000	26.69				19.92				
#2	750	20.13	2.98	60.15	179	17.49	3.45	36.72	126	42
#3	500	13.33				-0.7				
#1	500	13.38				18.20				
#2	500	13.38	2.97	40.14	119	18.20	2.25	54.60	123	-3,2
#3	500	13.38				18.20				

5. Conclusions and Future Work

It is concluded that module integrated QR ZVS SEPIC converter may increase the energy capture from photovoltaic system under partially shaded condition. Two different simulations are presented. One of them is for converter design in order to verify mathematical analysis. The other one is for use of DMPPT architecture to analysis system waveforms and measurements. The converter is capable of operating both below and above the input module voltage. It is also obtain that the converter is more flexible for shaded modules. The generated power in DMPPT architecture is higher than conventional architectures when part of the system is shaded.

Hardware of converters will be built and measurements will be done as future work. Then, converters will be connected series and field experiments will be done to verify DMPPT architecture simulation results. Microcontroller based control system is also be designed to control converters and string voltage.

6. References

[1] G. R. Walker, J. Xue and P. Sernia,"PV string per-module maximum power point enabling converters," *Australian Universities Power Engineering Conference, 2003.*

[2] G. R. Walker and P. C .Sernia,"Cascaded DC-DC converter connection of photovoltaic modules," *IEEE Transactions on Power Electronics*, vol.19, no.4, pp. 1130-1139,July 2004

[3] G. R. Walker and J. C. Pierce, "Photovoltaic DC-DC module integrated converter for novel cascaded and bypass grid connection topologies- design and optimization," *IEEE Power Electronics Specialists Conference*, 2006 Record, June 2006

[4] T. Shimizu, M. Hirakata, T. Kamezawa and H. Watanabe, "Generation control circuit for photovoltaic modules," *IEEE Transactions on Power Electronics*, vol.16, pp. 293-300, May 2001

[5] L. Linares, R. W. Erickson, S. MacAlpine, and M. Brandemuehl, "Improved energy capture in series string photovoltaics via smart distributed power electronics," *Twenty-Fourth Annual IEEE Applied Power Electronics Conf. and Exposition APEC 2009*, pp. 904-910, 2009

[6] R. W. Erickson, A. P. Rogers "A microinverter for building integrated photovoltaics," *Twenty-Fourth Annual IEEE Applied Power Electronics Conf. and Exposition APEC 2009*, pp. 904-910, 2009

[7] F. Lu, B. Choi, and D. Maksimovic,"Autonomous control of series connected low voltage photovoltaic microinverters" *Control and Modelling for Power Electronics(COMPEL),*

[8] Y. Fang, and X. Ma, " A novel pv microinverter with coupled inductors and double boost topology", *IEEE Transactions on Power Electronics*, vol.25, no.12, pp. 3139-3147, Dec 2010

[9] R. C. N. Pilawa-Podgurski, and D. J. Perreault, "Sub-module integrated distributed maximum power point tracking for solar photovoltaic applications," IEEE Energy Conversion and Exposition, pp.4776-4783, Sept. 2012

[10] M. K. Kazimierczuk, and D. Czarkowski, "*Resonant Power Converters*", 2nd. ed., A John Wiley&Sons, Inc., Publication, 2011

[11] K. H. Lıu, F. C. Lee, "Zero voltage switching technic in DC/DC converters," *IEEE Transactions on Power Electronics*, vol.5, no.5 , pp. 293-300, July 1990

[12] W. A. Tabisz, P. Gradzki, and F. C. Lee, "Zero voltage switched quasi resonant buck and flyback converter-Experimental results at 10MHz" *IEEE Transactions on Power Electronics*, vol.4, no.2 , pp. 194-204, Apr. 1989

[13] K. Liu, R.Oruganti, and F.C. Lee, "Quasi-resonant converters –Topologies and charesteristics" " *IEEE Transactions on Power Electronics*, vol.2, no.1 , pp. 62-71, January 1987