A High Bandwidth, Low Noise Preamplifier Using Active Inductor Load

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Abstract

In this paper, a high-speed preamplifier is designed to be applied in serial link transceiver. The proposed structure has high gain, low power, high bandwidth and low input-referred noise voltage. In addition, this structure is simple and totally on chip. Since this circuit is usually used in the first stage, the noise consideration is very important and must be investigated carefully. The circuits are designed in differential mode to eliminate the differential noise of transmission lines. In order to increase the bandwidth, a capacitor and an active inductor are added to the circuit. The proposed preamplifier is simulated in 180nm CMOS technology. The power consumption of proposed preamplifier is 3.6 mW with 1.8 V power supply. The unity gain frequency of proposed preamplifier is 19.3GHz with a phase margin of 85 degrees. The total equivalent input noise is 718 μ $\frac{v^2}{Hz}$ .Finally the Figure of Merit(FoM) of this preamplifier is 10.12MHz/μA

1. Introduction

Preamplifier stage amplifies the input signal for the next stage to modify the input sensitivity of the next stage. They are widely used in serial link transceivers and ADCs. One of the main blocks in serial link transceivers is preamplifier. As high-capacity transmission rate increases, high-speed serial links become more attractive than parallel links in fast wire-line transceivers. They can reduce cost, the number of cables and in count of output drivers [1]. Power efficiency is an important factor in serial link transceivers. Attaining a power efficiency of 1mW/Gb/s in wireline transceivers for operating at tens of gigabits per second is difficult [2]. At Transmitter side, the serial bits are transmitted towards receiver through a line one by one and placed side by side. The most challenging task in design of these serial link transceivers is designing a low noise preamplifier circuit with high gain and high bandwidth. Shunt-peaking method is an excellent technique to extend the preamplifiers bandwidth [3]. In this method, with an inductor in series with a resistor as load, the bandwidth of circuit is enhanced. Due to a large chip area of inductors, active inductors are used in some papers [4]. In [5][6] a preamplifier with active inductor load is designed. By using a large resistor as active inductor gate resistance, the locations of zero and poles are adjusted to obtain high gain and approximately high bandwidth. However, the bandwidth of this circuit is not high enough. In addition, the total noise, which is generated by several transistors in the circuit is considerable.

The preamplifier circuit is also used widely in Analog to Digital Converters (ADCs). Comparators are the main limiting block of ADC. One of the important blocks in Comparators, is preamplifier stage. With an increment in the minimum input signal, the comparator can take proper decision.

In [7] a low-noise preamplifier is designed to use in ADCs. This circuit is designed with a very low power consumption. However, the values of phase margin and gain bandwidth product are low.

In this paper, a new preamplifier, suitable for serial link transceivers, is proposed. The proposed circuit is designed with only 8 transistors. Therefore, the total input refereed noise of the circuit is considerably low. In addition, by using a special kind of active inductor as a load in the circuit, a very high gain bandwidth product is obtained. This design is accomplished in CMOS 180nm technology. Section 2 describes the proposed circuit design of the preamplifier for high speed transceivers. Simulation results from HSPICE tool using 180nm TSMC technology with a power supply of 1.8V is inducted in section 3. Finally, conclusions are presented in Section 4.

2. Proposed Circuit Design of Preamplifier

In design of serial link receiver, the main building block is its input stage. This input stage is commonly known as preamplifier or sense amplifier. The main task of the serial link receiver is to receive and amplify the input signal.

A simple conventional differential preamplifier is shown in Fig. 1. Vi1 and Vi2 are input differential signal that are received from transmitter side. Output dominant pole and low frequency gain in this circuit are;

$$\mathrm{s_p} = \frac{-1}{\mathrm{R_o C_o}} \ , \tag{1}$$

$$A_{v_{dc}} = g_m R_o \ , \tag{2}$$

where $\mathrm{C_o}$, R_o are equivalent capacitance and resistance at the output node and g_m is transconductance.

In this circuit, there is a tradeoff between gain and bandwidth. Since the value of resistance and capacitance at the output node are low, based on Equation (1), the dominant pole and bandwidth increase. However, with respect to Equation 2, the value of Gain decreases simultaneously.

In [8], according to Fig. 2, two inductors are added to the circuit to obviate this tradeoff. In this case, the Gain value is obtained as follows,

$$\mathrm{A_V} = g_m \left[\frac{1}{\mathrm{sC_o}} || (\mathrm{sL} + \mathrm{R_o})\right] \tag{3}$$

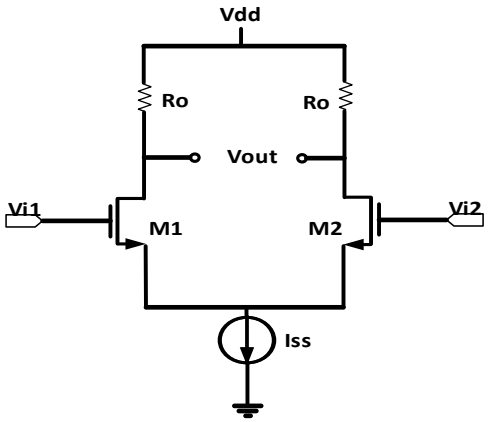


Fig. 1. Conventional differential preamplifier

This circuit has one zero and two poles. As follows;

$$s_z = \frac{-R_o}{L} \tag{4}$$

$$s_{p1} = \frac{R_o}{2L}\left[-1 + \sqrt{1 - \frac{4L}{C_0 R_0^2}}\right] \tag{5}$$

$$s_{p2} = \frac{R_o}{2L}\left[-1 - \sqrt{1 - \frac{4L}{C_0 R_0^2}}\right] \tag{6}$$

If the value of Ro and L parameters are selected carefully, sp and sz can cancel each other.

The value of total output admittance (Y) is given as bellow [8];

$$Y = \frac{1}{R_o + j\omega L} + j\omega c = \frac{1}{R_o + \frac{L^2\omega^2}{R_0}} + j\omega\left(c_0 - \frac{L}{R_0^2 + L^2\omega^2}\right) \tag{7}$$

If L is high, the effective admittance become inductive instead of capacitive. Therefore, the first zero will be shifted to very low frequency. Therefore, the bandwidth can be increased considerably. However, a high inductance will occupy a large chip area.

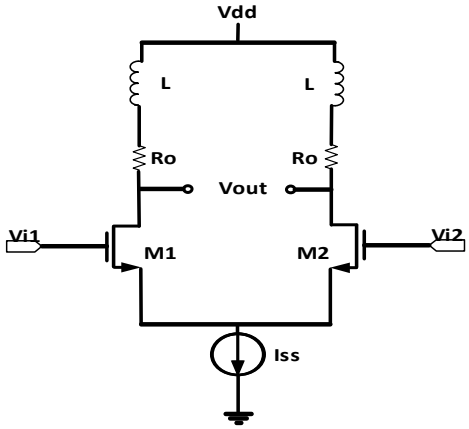


Fig. 2. Preamplifier circuit with inductor [8]

Fig. 3 (b) shows an active inductor [4] which can be used to solve the above problem.

The equivalent resistance of the circuit can be shown by Eq.8;

$$z_o = \frac{\frac{1}{R_f} + s(c_{gs} + c_{gd})}{(g_m + sc_{gs})\left(\frac{1}{R_f} + sc_{gd}\right)} \tag{8}$$

This circuit has two poles and one zero, as be low;

$$s_z = \frac{-1}{R_f(c_{gs} + c_{gd})} \tag{9}$$

$$s_{p1} = \frac{-g_{mp}}{c_{gs}} \tag{10}$$

$$s_{p2} = \frac{-1}{R_f c_{gd}} \tag{11}$$

According to Eqs. 9 and 11, with a very high resistance (R_f), the second pole and zero are transferred to the low frequency values. Therefore, Simultaneous zero and pole can be canceled.

However, in CMOS technology, implementing a very high resistance value, in order of tera-ohm is a very difficult task. In [5][6] a new preamplifier circuit(Fig.3(c)) is introduced to solve this problem. As indicated in Fig.3(c), this circuit uses a combination of cross-over transistors in parallel with diode connections to achieve a high resistance. The value of equivalent resistance in gate of transistor Mn of Fig.3 (c) is;

$$z_f = \frac{1}{g_{m_{p_1}} - g_{m_{p2}}} \tag{12}$$

As can be seen if the transconductance of transistors Mp1 and Mp2 are chosen carefully, infinite resistance is obtained. However, due to the variations of the value of gm with transistors voltage headroom, process and temperature, adjusting an accurate of gm will be very difficult. It means, the equivalent resistance is not high enough and the bandwidth of this circuit is achieve as 95MHz. Fig.4 indicates the proposed active inductor which resolves the above limitation. In proposed circuit, transistor Mn is biased to work in cutoff region, provides an extremely high resistance between its source and drain.

Considering the value of Mn drain-source resistance as infinity, the equivalent resistance of Fig.4 can be shown by the Eq.13;

$$z_o = \frac{\left(1 + \frac{c_{gs_p}}{c_{gd_p}}\right)}{g_{mp} + sC_{gs_p}} \tag{13}$$

The above transfer function has one pole as bellow;

$$s_p = \frac{-g_{mp}}{c_{gs}} \tag{14}$$

Eq.13 is a one-pole transfer function. It means that the values of first pole and first zero in Eq.9 and Eq.11 are canceled. The other pole is occurred at high frequency. Therefore, the bandwidth of the circuit increases significantly.

Fig. 5 shows the proposed design of preamplifier circuit which is first stage of serial link receiver circuit. This circuit includes two transistors M1 and M2 to amplify the input signal, two transistors M7 and M8 as the current source, capacitor C_p, two active inductors and two capacitors as capacitance load.

The n-channel input differential pair has two differential inputs Vi1 and Vi2 with 180 degrees Phase difference.

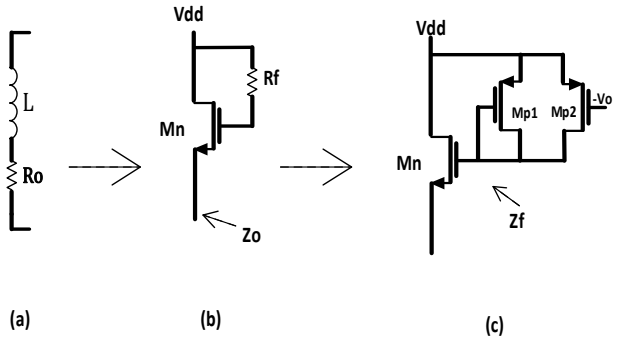


Fig .3. (a) An inductor series with resistor as load [8] (b) an active inductor load [4] (c) a modified active inductor load [5][6]

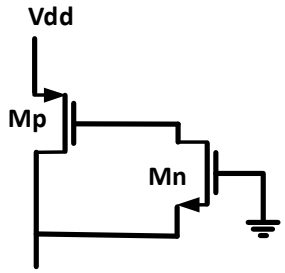


Fig.4.proposed active inductor load using concept of very high resistance

The size of M1,2 are set by considering the differential amplifier's transconductance and the input and output capacitance. The size of M3,4 are set by considering the active load works perfectly and saturation region. Biasing circuit is added in such a way that the current of current source become about 1mA. The gain of this stage can be expressed as;

$$A_V = \frac{-z_0}{\left(r_{o_{7,8}} || \frac{1}{s(2C_p + C_{gd_{7,8}} + C_{gs_{1,2}})} + \frac{1}{g_{m1,2}}\right)} \quad (15)$$

To extended bandwidth, the capacitor C_p is added to the circuit to increase bandwidth by adding a zero.

Relations of poles and zero of the equivalent of Fig.5 circuit are;

$$s_z = \frac{-1}{r_{o_{7,8}}(2C_p + C_{gd_{7,8}} + C_{gs_{1,2}})} \quad (16)$$

$$s_{p1} = ([-(C_{gd_{3,4}} C_{gs_{3,4}}(1 + g_{m1,2} r_{o_{7,8}}) + (2C_p + C_{gd_{7,8}} + C_{gs_{1,2}}) r_{o_{7,8}} C_{gd_{3,4}} g_{m3,4}) + \sqrt{\left(C_{gd_{3,4}} C_{gs_{3,4}}(1 + g_{m1,2} r_{o_{7,8}}) + (2C_p + C_{gd_{7,8}} + C_{gs_{1,2}}) r_{o_{7,8}} C_{gd_{3,4}} g_{m3,4}\right)^2 - 4(C_{gd_{3,4}} g_{m3,4}(1 + g_{m1,2} r_{o_{7,8}})(C_{gd_{3,4}} C_{gs_{3,4}} r_{o_{7,8}})(2C_p + C_{gd_{7,8}} + C_{gs_{1,2}}))} \times \frac{1}{2C_{gd_{3,4}} C_{gs_{3,4}} r_{o_{7,8}}(2C_p + C_{gd_{7,8}} + C_{gs_{1,2}})} \quad (17)$$

$$s_{p2} = ([-(C_{gd_3} C_{gs_3}(1 + g_{m1,2} r_{o_{7,8}}) + (2C_p + C_{gd_{7,8}} + C_{gs_{1,2}}) r_{o_{7,8}} C_{gd_{3,4}} g_{m3,4}) - \sqrt{\left(C_{gd_{3,4}} C_{gs_{3,4}}(1 + g_{m1,2} r_{o_{7,8}}) + (2C_p + C_{gd_{7,8}} + C_{gs_{1,2}}) r_{o_{7,8}} C_{gd_{3,4}} g_{m3,4}\right)^2 - 4(C_{gd_{3,4}} g_{m3,4}(1 + g_{m1,2} r_{o_{7,8}})(C_{gd_{3,4}} C_{gs_{3,4}} r_{o_{7,8}})(2C_p + C_{gd_{7,8}} + C_{gs_{1,2}}))} \times \frac{1}{2C_{gd_{3,4}} C_{gs_{3,4}} r_{o_{7,8}}(2C_p + C_{gd_{7,8}} + C_{gs_{1,2}})} \quad (18)$$

The value of C_p is chosen accurately. Therefore, the value of s_z and s_{p1} will cancel each other.

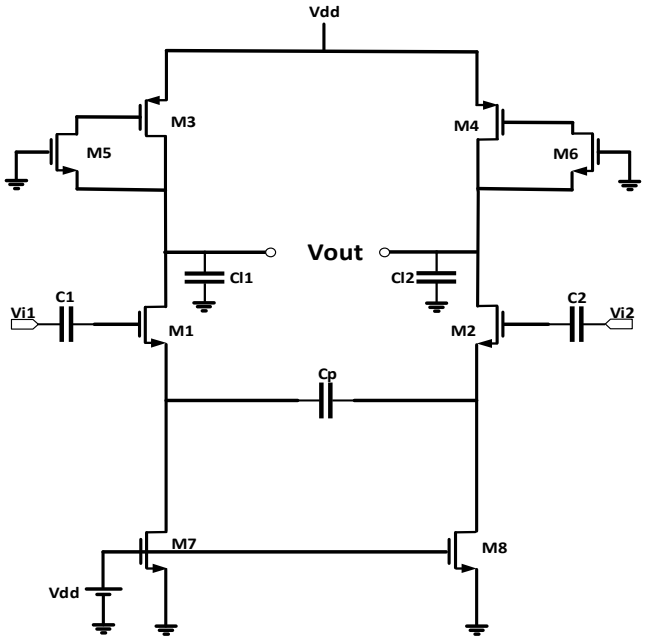


Fig. 5. Schematic diagram of proposed preamplifier

The operating point and values of transistors aspect ratio are given in table 1. In all of the relations and circuits, $C_{l1,2}$ are the output capacitances at the output node. The values of transistors aspect ratio are given in Table 1.

Table 1. Operating point and aspect ratio of transistors in Fig. 4

Transistors	W/L (μm/μm)	I_D (μA)	gm (A/V)
M1,M2	29/0.18	953	8m
M3,M4	9/0.18	953	2m
M5,M6	0.3/0.18	≈ **0**	≈ **0**
M7,M8	22/0.18	953	283μ

3. Simulation Results

The proposed circuit of the preamplifier is simulated in 180nm TSMC CMOS technology using HSPICE tool. The results of the simulation of proposed circuit are shown in Fig.6. As shown in Fig.6 (a), Since the bandwidth is 4.3GHz and the gain value at

this frequency is about 4.5 (13dB), the value of gain bandwidth product is 19.3GHz. The Phase Margin (P.M.) of proposed preamplifier is shown in Fig.6(b). As indicated in this figure, Phase Margin is about 85 degrees.

The most important noise factor in high speed amplifiers is the thermal noise. The amount of input refeered thermal noise in the proposed amplifier is calculated as follows.

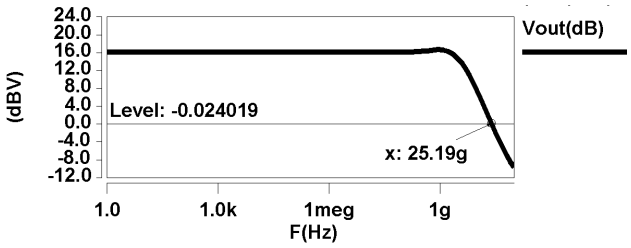
$$\overline{v_{n_{in}}^2} = 4kT\gamma\left(\frac{2r_c r_{o_{7,8}}}{2r_{c+}r_{o_{7,8}}}+\frac{1}{g_{m1,2}}\right)^2\left[g_{m1,2}+\frac{1}{r_{c_{l1,2}}}+g_{m3,4}+\left(g_{m7,8}+\frac{1}{2r_c}\right)\left(\frac{2g_{m1,2}r_c r_{o_{7,8}}}{2g_{m1,2}r_c r_{o_{7,8}}+2r_c r_{o_{7,8}}}\right)\right] \quad (19)$$

Where, γ , T and k are thermal noise coefficient which depends on the channel length modulation and effective mobility, temperature in kelvin and Boltzmann constant respectively[9]. r_o, r_c and r_{c_l} are input resistance of each transistors, capacitors C_p and C_l respectively. In proposed preamplifier the value of $g_{m1,2}$,the transconductance of input differential pair, is high. Therefore, according to Eq.19, the thermal noise is minimized. The input noise of the preamplifier is shown in Fig. 6(c). accordingly, this preamplifier has a very low noise in low frequency range, and is approximately zero at frequencies higher than 100Hz.The FoM according to GBW/I_q relationship [11] is 10.12MHz/μA that GBW and Iq are Gain × Bandwidth and quiescent supply current respectively.

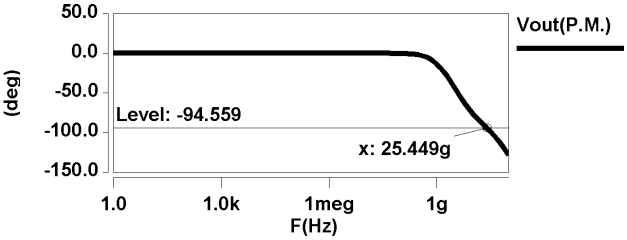
Table 2 present a comparison between different preamplifiers. The circuits given in [5], [6] have a low power consumption and a high gain, but the bandwidth of these circuits is low. Except for the case of [12], the value of gain bandwidth product in the proposed circuit is higher than that of other circuits. However, since [12] has a passive inductor, the power consumption of this circuit is high and the circuit should also be used out of the chip.

4 . Conclusion

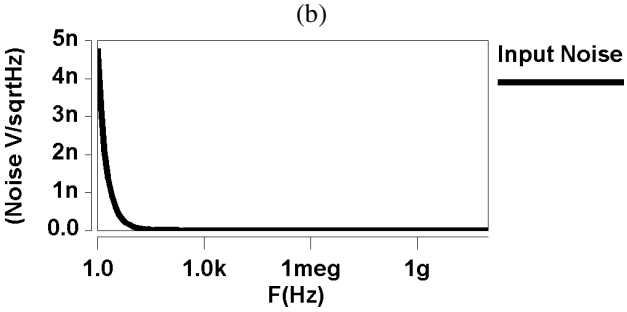
This paper presents a low noise, high bandwidth, high gain and low power preamplifier. The proposed preamplifier achieves a unity gain frequency of 19.3GHz and maximum gain of 16.5dB with a phase margin of 85 degrees. Using a large resistance, as active inductor gate resistance, bandwidth value is extended considrably while the gain value remains unchanged. The preamplifier is designed using 180nm TSMC CMOS technology with HSPICE tools. The overall power consumption of the circuit is 3.6mW and total equivalent input noise is 718 μv^2/Hz.



(a)



(b)



(c)

Fig. 6. Simulation result of gain (a) phase margin (b) and input noise (c) of proposed preamplifier.

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Table 2. Simulation Results Comparison Between Different Preamplifiers

Ref.	Supply Voltage	Technology	Bandwidth (-3 dB)	Gain× Bandwidth	Power	On chip?	Gain
[5],[6]	1.8 V	180nm CMOS	95 MHz	12 GHz	1.39mW	yes	41.8 dB
[10]	1.8 V	180nm CMOS	40-1200MHz	4.1GHz	14.4mW	yes	24.3 dB
[12]	2.5 V	180nm CMOS	19GHz	24GHz	111mW	no	11dB
This work	1.8 V	180nm CMOS	4.3GHz	19.3GHz	3.6mW	yes	16 dB