A Novel Ultra High Speed and Low Power Phase Detector using Carbon Nanotube Field Effect Transistors

Noushin Ghaderi[1], Mahboubeh Alidadi-Shamsabadi

Faculty of Engineering, Shahrekord University, Shahrekord, Iran
[1]ghaderi.nooshin@eng.sku.ac.ir

Abstract

As the scaling of conventional silicon transistors moves towards its limiting value, designers become interested to exploit novel nanotechnologies. A carbon nanotube field effect transistor (CNFET) is a potential alternative device that avoids most of the physical limitations. In this paper, a high speed, low power, high precision and extensive range CNFET based phase detector (PD) is presented. The sequential circuits and the feedback path are not used in the proposed PD to obtain the best speed. In addition, by employing a new method, the dead zone and missing edge problems are completely solved in the proposed PD without any need to apply extra delay cells. Therefore, the delay time mismatch is omitted in the proposed circuit. Simulation results using HSPICE based on the CNFET model show that the proposed PD consumes only 24.5 µw power and is much faster than the ones proposed in the previous works.

1. Introduction

In the last decades, silicon-based integrated circuit technology has experienced tremendous growth due to the scaling of device dimensions. However, the size reduction of metal oxide semiconductor field effect transistors (MOSFETs) below a few tens of nanometers decreases their performance because of the non-ideal phenomena such as gate oxide leakage, mobility degradation, and low "ON" current[1]. Researchers have currently focused on CNFETs as a promising alternative to MOSFETs in the nanoregime. CNFETs are novel nanoscale devices with high performance due to their premier electrical properties. Recently, some circuits like opamp[1], biosensor[2], ternary memory cell[3], and SRAM cell[4] have been modified using CNFETs. It seems that CNFETs can obtain superior "ON" current density, higher operation frequency, and considerably lower power consumption[5]. Thus, CNFETs are useful to design a high-speed circuit with low power consumption.

As the speed increases, a higher clock frequency is required. Phase-locked loops (PLLs) and delay-locked loops (DLLs) are widely used in modern communication systems to generate a clock signal which is synchronized with a reference clock. These circuits are commonly used in many applications such as clock/data recovery, frequency synthesis, and phase/frequency modulation. A phase detector (PD) is an essential functional block of a PLL, which is used to detect a phase error signal, and plays a key role in improving the speed of the PLL system. The outputs of PD are “UP” and “DN” signals that switch the current of a charge pump to adjust the control voltage of a voltage controller oscillator (VCO). Fig. 1 shows a well-known linear PFD architecture using D-type master-slave flip flops[6]. Conventional PDs have closed loop structures, as they are simple to design and do not have the dead zone problem. However, the speed of these systems is limited due to the use of a feedback path. Furthermore, some of the clock rising transitions, which overlap with the reset signal, will be missed and cannot be detected[7]. Until now, some circuits have been proposed to more quickly force the feedback path[8][9]. However, the feedback path, which causes a reduction in the speed, still remains in all of them. Therefore, by setting an open loop path and using CNFETs, a high speed and high efficiency PD can be designed.

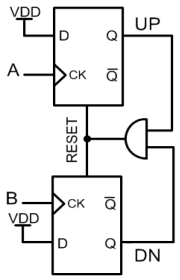

Fig. 1. Logic schematic of the conventional PD

In this paper, a simple and fast CNFET-based open loop PD is presented, which detects phase difference in a wide frequency range from 1 MHz to 12.5 GHz. Adjustable threshold voltage (Vth) is one of the most exciting features of CNFETs that is used to propose a simple PD with a few transistors in this paper. In the ordinary CMOS open loop PFDs, some delay cells must be added to solve the dead zone problem. Adding these delay cells will add some mismatch delay time to the circuit, which causes an extra jitter in the output [20][21]. This problem is completely solved in the proposed circuit by omitting the delay cells while taking advantage of adjustable threshold voltages of CNTFET transistors.

Section 2 presents a short description of the fundamental of CNFETs and introduces different kinds of them. The proposed open loop PD is discussed in Section 3. Section 4 reports simulation results and compares the proposed structure with the previous works. Finally, conclusions are provided in Section 5.

2. CNFETs

Carbon nanotubes (CNTs) are graphene strips rolled into a seamless, hollow cylinder[11]. The features of CNTs rely strongly on physical properties like their diameter, length, and chirality (direction of the graphene sheets). For instance, by varying an intrinsic bandgap, CNTs can be in single-walled (SWCNT) and multi-walled (MWCNT) geometries. Furthermore, SWCNTs could be either semiconducting or metallic based on their chirality[2]. Chirality vector is indicated by the positive integers (n1,n2). CNTs act as metallic if n1= n2

or $n_1 - n_2 = 3q(q \in z)$. Otherwise, the nanotube is semiconducting[12]. The diameter of CNTs is given by[13]:

$$D_{CNT} = \frac{a}{\pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} \approx 0.078\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (1)$$

Where $a = 2.49A°$ is the lattice constant. CNTs have superior properties such as near ballistic transport owning to ultra long mean free path for elastic scattering[14] that makes them a proper candidate for use in the channel region of FETs, named CNFETs[15].

In terms of the device operation mechanism, CNFETs can be divided into two groups of Schottky barrier CNFETs (SB-CNFETs) and MOSFET-like CNFETs[1]. SB-CNFET is fabricated using direct contacts of the metal with the semiconducting CNTs for source and drain regions and undoped semiconducting nanotube for the channel region. These devices show an ambipolar behavior that makes them unsuitable for use in conventional CMOS logic families[11]. The energy barrier at the Schottky barrier limits the transconductance of the CNFETs and decreases the Ion/Ioff ratio[16]. In MOSFET-like CNFET, intrinsic semiconducting CNTs are placed under the gate in the channel region and heavily doped CNTs are used for the source and drain regions. Unlike SB-CNFETs, they have unipolar characteristics and significantly higher Ion/Ioff ratio[11]. As a result, this type of CNFETs is more suitable for ultra high performance applications[3]. Therefore, in this paper, we focus on MOSFET-like CNFETs for the proposed design. The current-voltage characteristics of CNFETs are similar to those of MOSFETs. Thus, to turn on the CNFET, a threshold voltage should be defined. The threshold voltage of the CNFET can be approximated to the first order as the half-bandgap that is proportional to the inverse of the diameter of CNT and can be expressed as[10]:

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}aV_\pi}{3eD_{CNT}} \approx \frac{0.43}{D_{CNT}}v \quad (2)$$

where a is the lattice constant, e is the unit electron charge, and $V_\pi = 3.3eV$ is the carbon $\pi - \pi$ bond energy in the tight bonding model. This geometry-dependent threshold voltage has been used to obtain CNFETs which are turned on at different voltages relying on their diameters.

3. Proposed CNFET-based PD

Thus far, various close loop and open loop PDs have been implemented in different logic styles[17-21]. Although these structures have tried to solve the problems of dead zone and missing edges in PDs, they could not significantly improve the operation frequency and power consumption. All the previous PDs have been implemented using different kinds of CMOS technology.

In this section, a novel open loop PD with high operation frequency and low power consumption is illustrated based on a carbon nanotube technology. As shown in Fig. 2, the proposed design is constructed in three stages. The first stage generates a signal which is a complement of the lagged input ($\overline{Lag}$) using two capacitors and two CNFETs. According to the input signal values, the capacitors produce 3 logic levels, 0, VDD/2, and VDD at the gates of T_1 and T_2 (G_1 node). The threshold voltages of T_1 and T_2 are regulated as follows. The "$\overline{Lag}$" signal will be high when both of the inputs are low (logic level = 0) and it will be low if both of the inputs are at a high value (VDD level). In the rest of the input states, the output does not change. For better evaluation, different states are tabulated in Table 1.

Table 1. Different states of the first segment of the Proposed PD

A	B	Logic level of G_1	T_1	T_2	Lag not
0	0	0	Off	On	1
1	0	VDD/2	Off	Off	Previous state
1	1	VDD	On	Off	0
0	1	VDD/2	Off	Off	Previous state

The second stage implements "$\overline{UP}$" and "$\overline{DN}$" by using two NAND gates. "$\overline{UP}$" will be set to zero when both of its inputs ($\overline{Lag}$ and A) are high. Otherwise, it will become high. "$\overline{DN}$" signal is generated in a similar manner. Finally, two inverters are needed to implement "UP" and "DN" signals with sharp edges, which are used in the charge pump circuit to produce a voltage or current as a control signal to VCO. Only 10 transistors have been used to design the proposed PD that is unprecedented in the previous works. In addition, these transistors are much faster and consume less power than MOSFETs. Figure 2 indicates the diameter of each transistor as computed and written by Eq. 2.

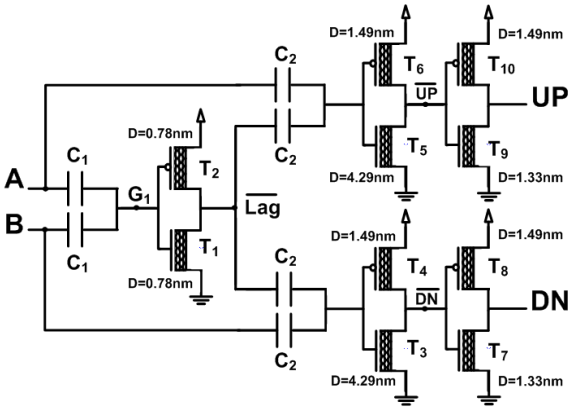

Fig. 2. Proposed CNFET-based PD

Production of "UP" and "DN" signals is illustrated in Fig. 3. Initially, both "A" and "B" signals are set to a minimum value (A=0 and B=0). Therefore, according to Table 1," $\overline{Lag}$ " signal is set to VDD level and, subsequently, "UP" and "DN" signals will be zero. When the rising edge of "A" occurs, "$\overline{Lag}$" and "DN" signals will remain in the previous state and "UP" signal will be set to the high value. After the rising transition on "B", T3 will turn on and "DN" signal will be set to the high level.

After a specific time delay, the "$\overline{Lag}$" signal will change its state. This time delay is produced due to the capacitors in the

proposed structure, which is needed to produce "DN" signal and earn enough time for output signals to reach a logical level in small phase differences. "UP" and "DN" signals will be reset to "0" when the falling edge of "$\overline{Lag}$" happens. As is shown, "UP" and "DN" signals overlap with each other, which makes equal charge and discharge currents pass through the filter capacitor. In this way, the dead zone of the proposed structure will be zero, which is very desirable for high speed systems. In the previous open loop structures[20], the delayed version of the input signals was used to overcome the dead zone problem, which not only imposed some additional circuits, but also caused the jitter and mismatch problems to be created in the output pulses of VCO. In the proposed circuit, due to applying the benefits of adjustable threshold voltages, which can be accomplished just in the CNTFET process, the above problem is omitted as a result of omitting the delay circuits.

In the next step, "A" becomes zero, while "$\overline{Lag}$" remains in the previous state. Then, "B" goes low and "$\overline{Lag}$" will be set to "1".

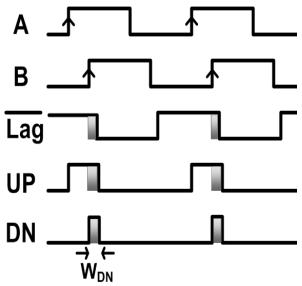

Fig. 3. Waveforms of the proposed PD

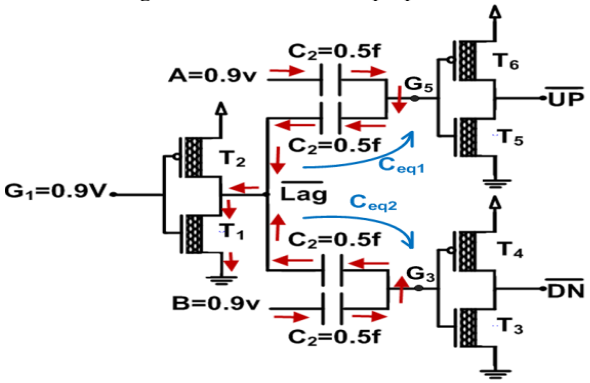

Fig. 4. The discharge paths of the lag not node, which are shown with red vectors

As previously mentioned, the pulse width of "DN" signal (W_{DN}) is related to the discharge time of the "$\overline{Lag}$" node capacitor (Fig. 4). "UP" and "DN" signals remain in their previous states until the voltage of G_3 and G_5 nodes is reduced to a value which is less than the threshold voltages of T_3 and T_5. Then, they will be turned off and "UP" and "DN" signals will be set to zero. The discharge time and, subsequently, "W_{DN}" are estimated as follows. As shown in (3), the drain-source resistance of T_1 is approximately equal to the resistance of CNTs placed in the drain, source and channel regions. The capacitance of T_1 is negligible in comparison with the connected capacitors (C_2). The equivalent capacitance of the "$\overline{Lag}$" node is equal to 0.5 fF. The time needed to discharge the "$\overline{Lag}$" node capacitance from VDD to 0.368 VDD is equal to time constant (τ) (Eq. (3)). It means that this time is needed to turn off T_3 and T_5 and turn on T_4 and T_6.

$$R_{eq} \approx \frac{R_{CNT} * 96nm}{Tubes}, R_{CNT} \approx 3.3\frac{K\Omega}{nm}, \text{Tubes} = 5 \rightarrow R_{eq} = 63.36K\Omega,$$
$$C_{eq} \approx C_{eq1} \| C_{eq2}, C_{eq1} = C_{eq2} \approx \frac{C_2}{2} = 0.25fF \rightarrow C_{eq} \approx 0.5fF,$$
$$W_{DN} \approx \tau, \text{Where } \tau = R_{eq} * C_{eq} \rightarrow W_{DN} \approx 31.68ps. \quad (3)$$

Where Tubes is the number of CNT tubes in the device; also, R_{eq} and C_{eq} are the equivalent resistor and capacitor of the "$\overline{Lag}$" node, respectively.

4. Simulation Results and Design Comparison

The HSPICE circuit simulator is used to simulate the proposed PD. The standard model presented in [16] is also used to simulate enhancement-mode unipolar MOSFET-like CNFETs, in which each transistor may include several CNTs as its channel. The important parameters of the top gate CNFET standard model are physical channel length (L_{ch}=32nm), length of doped CNT source-side extension region (L_{ss}=32nm), length of doped CNT drain-side extension (L_{dd}=32nm), width of metal gate (W_{gate}=6.4nm), distance between the centers of two adjacent CNTs within the same device (Pitch=20nm), number of tubes in the device (Tubes=1), thickness of high-k top gate dielectric material (T_{ox}=4nm), dielectric constant of high-k top gate dielectric material (K_{gate}=16), coupling capacitance between the channel region, and substrate (C_{sub}=20pF/m), which are shown in Fig. 5. The default value of each parameter is written inside the parenthesis.

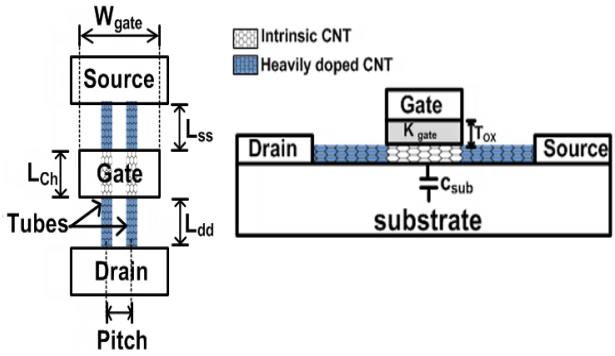

Fig. 5. Presentation of the modeled CNFETs and relevant parameters

The proposed PD is simulated at room temperature and 0.9 volt supply voltage. SPICE simulation results presented in Fig. 6 show that "UP" and "DN" signals are made with high accuracy, while the operation frequency is very high. The pulse width of "DN" is about 29.7ps, which is approximately equal to what is theoretically estimated (31.68ps). "UP" and "DN" signals overlap with each other and simultaneously come down. In this way, the dead zone will be zero, which makes it suitable to be used for applications with high speed and high accuracy. Assuming that "A" and "B" signals have similar frequencies

(F_A= F_B) and their duty cycle is 50%, the maximum frequency (F_{max}) of the inputs should be chosen so that their pulse width is greater than the pulse width of "DN" signal (W_{DN}). If F_{max} is more than the mentioned value and the phase difference of the inputs is close to 180º, the "DN" signal does not have enough time to change its state. Therefore, the maximum frequency is given by:

$$F_{\max} = \frac{1}{2 * W_{DN}} = \frac{1}{2 * 29.7ps} = 16.8GHz \quad (4)$$

To ensure that the circuit works properly, the operating frequency is selected as 12.5 GHz, which is less than the maximum frequency theoretically determined.

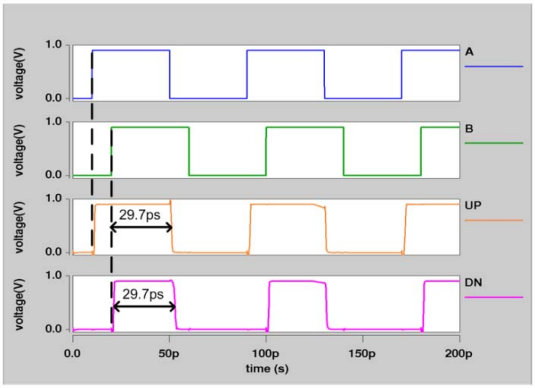

Fig. 6. Waveforms of the designed PD when the input frequency is 12.5GHz and two inputs are 45 ºout of phase.

The input, output (I/O) characteristics of PD at the frequencies of 3GHz, 10GHz, 11.1GHz, and 12.5GHz are displayed in Fig. 7, where the x axis illustrates the phase difference of "A" and "B" signals and the y axis represents the average values of the difference between "UP" and "DN" signals. The region around zero, surrounded by the circle, shows that PD behaves linearly in small phase differences, even at very high frequencies (12.5GHz). In this way, the proposed structure has low jitter after locking the PLL. As the phase difference increases, the transitional curves become nonlinear, but they hold correct polarity. This structure can detect the phase difference in a wide frequency range from 1MHz to 12.5GHz and consumes only 24.5µw when working at 12.5 GHz.

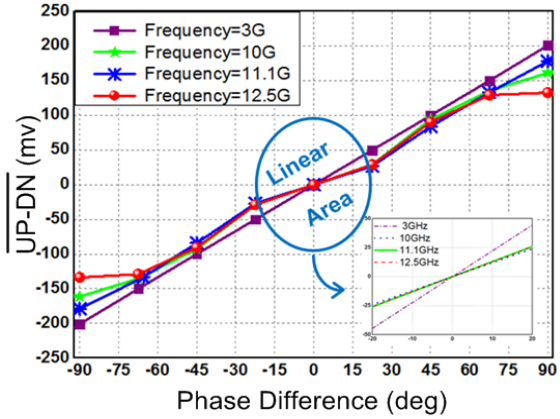

Fig. 7. I/O characteristics of the proposed PD

To highlight the advantages of the proposed PD, a comparison is made with the previous works, which is indicated in Table 2. As is shown, the operation frequency is fastest and the average power dissipation of the proposed PD is less than that of all the previous structures.

5. Conclusion

In this paper, a novel low power open loop PD was proposed. The PD used CNFETs and capacitances as a substructure, resulting in considerable improvement in the speed and power consumption. In addition, in proposed PD, the problem of mismatch delay time and jitter, which is due to the addition of a number of delay cells to the circuit, is completely solved by omitting the delay cells while taking advantage of adjustable threshold voltages of CNTFET transistors.

Simulation results demonstrated that the operating frequency of the presented CNFET-based PD ranged from 1MHz to 12.5GHz and consumed only 24.5µw at 12.5GHz. It could also detect very small phase differences with high accuracy and completely solve the dead zone and missing edge problems, which made it preferable to be used for fast lock, low output jitter, and high operating frequency PLLs.

Table 2. Proposed PD performance summery and comparison

References	Technology	Structure	Power	Max Freq.
[17]	CMOS 250nm	Close loop	1.4mw@ 500MHz	1.5GHz
[18]	CMOS 130nm	Close loop	37µw @ 1GHz	2GHz
[19]	CMOS 180nm	Close loop	1.56mw@ 500MHz	2.3GHz
[20]	CMOS 180nm	Open loop	0.4mw@ 8GHz	8GHz
This work	CNT 32nm	Open loop	24.5µw@ 12.5GHz	12.5GHz

6. References

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