Design and Implementation of Phase-Shifted Full-Bridge Converter with a Current Doubler for HV to LV Battery Charger in EVs

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Abstract

Growing demand for electrical vehicles has caused an increase in the usage of power electronic converter units. One of them is high-voltage to low-voltage converter. Soft switching converters which have zero voltage or zero current switching capability have come to the forefront to reach higher efficiency. In this study, a phase shifted full-bridge converter with current doubler rectifier stage is selected, studied and implemented. Design calculations and selected components regarding to these calculations for a 3 kW rated converter for wide input and output voltage range is provided. Simulation model with the spice models of selected components is implemented in LTspice. Analytical results and their compatibility are verified with simulation and experimental results. The efficiency of 95.7% at 400 V input , 12 V output voltage, and 3 kW output power is achieved from simulation, while efficiency of achieved as 93.4% is achieved from the experiment.

1. Introduction

Global warming and the depletion of natural resources have become global issues in recent decades, resulting in the need to regulate petroleum-based fuel consumptions and carbon dioxide emissions. Accordingly, electrification solutions have been started with various eco-friendly vehicles such as hybrid electric vehicles (HEV), plug-in HEVs (PHEV), mild HEVs (MHEV), and electric vehicles (EVs). Electric machines, energy storage devices, and power electronic converters associated with motor drives all play key roles with the continued development of these systems. Among them, HEVs and PHEVs require a high-voltage (HV) battery which has from 200 V to 800 V voltage level; in addition, most of the vehicle's electronic equipment requires a low-voltage (LV) battery which has a 12 V voltage rating for charging. In such vehicles, a power electronics-based DC-DC converter takes over the role of the belt-driven generator and supplies low voltage battery from high voltage battery [1, 2]. This converter is named as low voltage DC-DC converter (LDC) [3] or auxiliary power modules (APM) [4] in the literature. The general architecture of electrical vehicles with HV, LV batteries and converters is given in Fig. 1.

Converter is named as APM in this study. APM has to operate at a wide operating voltage range which depends on the HV and LV battery specifications in the vehicle. Moreover, its power changes according to auxiliary loads, such as the air conditioner, headlights, sound systems, lighting, electronic control units, wiper, window system, etc. [1]. The power requirement of the APM increases as additional features
and auxiliary hardware are added to the vehicle.

Design optimization of auxiliary loads of the APM has a significant impact on energy consumption and electric range due to continuous operation when the vehicle is in use. For this purpose, soft switched topologies could be selected. The soft switching technique helps to reduce switching losses by generating zero-voltage and/or zero-current situations for the power switch during switching. Thus, this feature reduces the switching stress over switch. Moreover, soft switching helps to get better EMI performance than hard switching operation. With the help of these features of soft switching, converters could operate at high switching frequency which enables to use of smaller-sized magnetic components. As a result of all these advantages, the efficiency and reliability of the converter increase [5]. Phase shifted full-bridge (PSFB) converter is the one of the converters which has zero-voltage switching (ZVS) feature with constant switching frequency, and without any additional auxiliary components or complex control circuit [6].

PSFB converter is used as a power supply topology that has high efficiency and power density from 500 W to 5000 W power rated applications requiring isolation between input and output [7]. ZVS is achieved by a suitable phase shift pulse width modulation (PWM) scheme with the usage of parasitic elements in the circuit which are transformer leakage inductance and output capacitance of switches C_{oss} [2].

The rectification side is also another important part of the converter, since the power of APM could be as high as a kilowatt scale with hundreds of amperes at output [3]. There are several studies as an example which designed for different power ratings as 2 kW [2], 3 kW [1], and 3.8 kW [8] as HV to LV battery charger in electric vehicle. Current doubler rectifier (CDR) is the most proper rectification configuration for high current applications since output current splitting into two. The advantages of CDR are conduction losses reduction, thermal management improvement, simpler transformer structure, and ripple current cancellation at the output [3, 9, 10].

In this study, a 3 kW PSFB converter with CDR for EV is simulated using LTspice. Information and principle of PSFB with CDR converter in given section 2. Design calculation steps and selected components are provided in section 3. Simulation results with real component models are given in section 4. Experimental results of implemented PSFB with CDR are given in section 5. The conclusion and future work are presented as a final section.

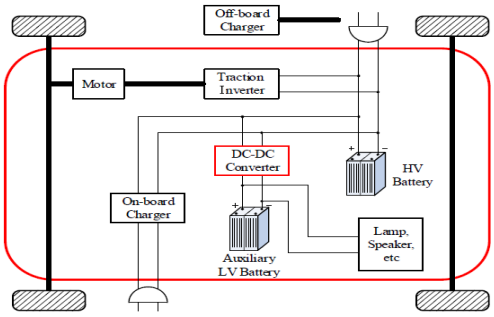

Fig. 1. General architecture of batteries and converters in EV [3]

2. Principle of PSFB with CDR Converter

PSFB with CDR converter is highly suitable for APM applications because of ZVS operation due to simplicity of both hardware and software. Moreover, CDR enable to operate with high current. PSFB with CDR combination circuit schematic is shown in Fig. 2.

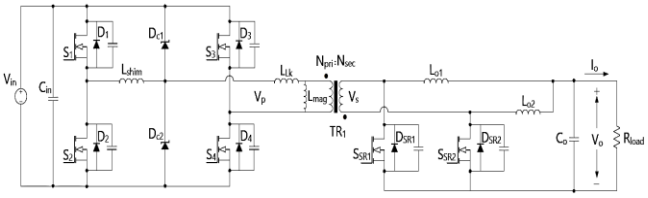

Fig. 2. Circuit representation of PSFB with CDR

Primary side switches which are S_1, S_2, S_3, and S_4 conduct almost 50% fixed-duty cycle, however, effective duty cycle is generated by the overlapped of S_1 and S_4, and S_2 and S_3. Deadtime has to be applied between S_1 and S_2, and S_3 and S_4 to prevent short circuit. ZVS could be achieved during this dead time with the help of resonance between output capacitances of S_1, S_2, S_3, S_4 and stored energy in shim inductor L_{shim} which helps to achieve ZVS operation for light load condition and transformer leakage inductance L_{lk}. Shim inductor causes to increase in the number of components, however, increases the overall efficiency of the converter. The same situation could be obtained with increasing of L_{lk}, yet that option causes to increase of voltage overshoot on the secondary side switches and decreases the efficiency. L_{shim} also contributes to voltage overshoot on the secondary side switches, nevertheless, D_{c1} and D_{c2} which are the clamping diode could overcome this problem by clamping this overshoot. Detailed analysis about this issue evaluated in [11].

L_{mag} is the magnetizing inductance of the transformer. S_{SR1} and S_{SR2} are the switches in the CDR at the secondary side. These two switches are switched in relation of primary side switches state. L_{o1} and L_{o2} are the output inductors. C_o and C_{in} are output and input DC-Link capacitor respectively.

3. Design Steps of PSFB with CDR Converter

One of the main important steps is calculating and selecting proper components for selected topology which is PSFB with CDR in this study. All analytical calculations are given step by step, yet first of all operating point specifications are given in Table 1.

Table 1. Operating condition intervals

Power Rating	3 kW
Input Voltage Range	240 V-475 V
Output Voltage Range	10.9 V-14 V
Output Current Range	214 A-275 A
Target Efficiency	95%
Switching Frequency	100 kHz

Input and output voltage, output current varies between shared intervals in Table 1. Thus, all calculated values and selected components have to satisfy the worst operating condition successfully. It is important to have feasible calculated values for circuit components, since components have to exist in the market or could be manufacturable in terms of electrical specification and physical dimensions.

3.1. Calculations Related with Switches

To begin with, current which flows through primary and secondary switches is calculated. The calculation of the current of primary switches requires to know the turns ratio roughly as a first step. If the maximum effective duty cycle D_{eff} is assumed as 45%, the turns ratio which is the primary side turns N_{pri} over the secondary side turns N_{sec} is calculated as around 7. I_o is output current. Primary side switches RMS current $I_{pri,rms}$ and secondary side switches RMS current $I_{SR,rms}$ are calculated by using Eq. 1-2. $I_{pri,rms}$ and $I_{SR,rms}$ are calculated as 13.90 A and 209.411 A respectively.

$$I_{pri,rms} = \frac{I_o}{2} \cdot \frac{N_{sec}}{N_{pri}} \sqrt{\frac{1}{2}} \tag{1}$$

$$I_{SR,rms} = I_o \sqrt{\frac{D_{eff}}{2} + \frac{1}{4}} \tag{2}$$

Other important parameter which is the voltage stress over primary and secondary switches. Maximum voltage stress on the primary side is equal to input voltage V_{in} which is 475 V. Primary side switch is selected as SiC MOSFET IMBG65R048M1H from Infineon. The voltage stress on the secondary side $V_{SR,stress}$ which depends on output voltage V_o and D_{eff} is calculated as in Eq. 3 [10]. According to the calculation $V_{SR,stress}$ is found as 66.67 V.

$$V_{SR,stress} = \frac{V_o}{D_{eff}} \tag{3}$$

With consideration of calculated values, the secondary side switch is selected as Si MOSFET IAUTN12S5N018G from Infineon.

3.2. Calculations Related with Transformer

One of main parameter of transformer is the turns ratio which has been calculated as 7 in section 3.1 as roughly. However, it has to be validated with consideration of voltage drop-over switches. After selecting both primer and seconder switches, voltage drops V_{Rdson} could be calculated with obtained RMS current I_{RMS} and on resistance of switch R_{dson} by Eq. 4.

$$V_{Rdson} = I_{RMS} \cdot R_{dson} \tag{4}$$

V_{in} is the input voltage. $V_{Rdson\text{-}pri}$ is the primary side switch voltage drop, $V_{Rdson\text{-}SR}$ is secondary side switch voltage drop. Maximum D_{eff} value is decided as 45% since, deadtime and duty cycle loss time have to be considered. The turns ratio of transformer is calculated as 7 according to Eq. 5.

$$\frac{N_{pri}}{N_{sec}} = \frac{(V_{in} - 2 \cdot V_{Rdson\text{-}pri}) \cdot D_{eff}}{V_o + V_{Rdson\text{-}SR}} \tag{5}$$

Magnetizing inductance of transformer L_{mag} is another important parameter of the transformer. It has to be sufficient to enable proper converter operation. On the other hand, wrong selected transformer in terms of L_{mag} causes efficiency drop and control problem. L_{mag} and magnetizing current ripple ΔI_{Lmag} are calculated in Eq. 6 and Eq. 7, respectively. L_{mag} is selected as 1.5 mH as a result of the calculation.

$$L_{mag} \geq \frac{V_{in} \cdot (1 - D_{eff})}{\frac{\Delta I_{Lo1} \cdot 0.5}{\frac{N_P}{N_S}} \cdot f_{sw}} \tag{6}$$

$$\Delta I_{Lmag} = \frac{V_{in} \cdot D_{eff}}{L_{mag} \cdot f_{sw}} \tag{7}$$

The primary side current of transformer $I_{TR\text{-}pri,rms}$ and secondary side current of transformer $I_{TR\text{-}sec,rms}$ have to be known to design the proper transformer during the prototyping stage. These values are calculated by Eq. 8 and Eq. 9.

$$I_{TR\text{-}pri,rms} = \frac{I_o}{2} \cdot \frac{N_s}{N_p} \tag{8}$$

$$I_{TR\text{-}sec,rms} = \frac{I_o}{2}\sqrt{2 \cdot D_{eff}} \tag{9}$$

Peak current $I_{TR\text{-}pp}$ and minimum current $I_{TR\text{-}pm}$ which flows over the primary side of the transformer is calculated as in Eq. 10-11 [12]. These current values are also important by reason of having an effect on another component parameter which will be calculated.

$$I_{TR\text{-}pp} = \left(\frac{P_{out}}{V_o \cdot \eta} + \frac{\Delta I_{Lo1}}{2}\right) \cdot \frac{N_s}{N_p} + \Delta I_{Lmag} \tag{10}$$

$$I_{TR\text{-}pm} = \left(\frac{P_{out}}{V_o \cdot \eta} - \frac{\Delta I_{Lo1}}{2}\right) \cdot \frac{N_s}{N_p} - \Delta I_{Lmag} \tag{11}$$

3.3. Calculations of Critical Timings

Duty cycle and deadtime calculation are highly important for operation of converter properly. D_{eff} has to be checked whether it satisfies the limit of D_{eff} with selected transformer turns ratio for operating condition intervals. Maximum D_{eff} value is calculated as 41.7% for 240 V as $V_{in,}$ 14 V as V_o , 214 A as I_o by Eq. 12.

$$D_{eff} = \frac{\frac{N_{pri}}{N_{sec}} \cdot (V_o + V_{Rdson\text{-}SR})}{(V_{in} - 2 \cdot V_{Rdson\text{-}pri})} \tag{12}$$

Deadtime T_D is another critical parameter to achieve ZVS and high efficiency. Resonant period T_r is the limitation for T_D as in Eq. 13. L_k is the summation of L_{shim} and L_{lk}. L_{lk} value is 700 nH which belongs to the designed transformer with the manufacturer which will be used in the future step that is prototyping. C_{TR} is transformer parasitic capacitance which could be neglected since quite small when compared with time related output capacitance of primer switches $C_{pri\text{-}coss(tr)}$. Resonant frequency f_r is calculated by Eq. 14 [10]. Pursuant to these calculations, T_D is selected as 100 ns.

$$T_D \geq {T_r}/{4} \tag{13}$$

$$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_k \cdot (2 \cdot C_{pri\text{-}coss(tr)} + C_{TR})}} \tag{14}$$

3.4. Calculations Related with Inductors

There are two different external inductors in PSFB with CDR converter. One of them is named as output inductor and other one is named as shim inductor.

First of all, target current ripple values on the output inductors ΔI_{Lo1} and ΔI_{Lo2} have to be selected to calculate the suitable inductance value for output inductors L_{o1} and L_{o2} as given in Eq. 15. The target ripple value is chosen as 40%. Afterwards, L_{o1} and L_{o2} are calculated by Eq. 16. T is the period of switching. The inductance value is selected as 2.5 µH.

$$\Delta I_{Lo1} = \Delta I_{Lo2} = \%Ripple \cdot \frac{I_o}{2} \tag{15}$$

$$L_{o1} = L_{o2} = \frac{1}{\Delta I_{Lo1}} \cdot V_o \cdot (1\text{-}D_{eff}) \cdot T \tag{16}$$

The current rating of L_{o1} and L_{o2} are half of the output current, since the rectification side configuration is a current doubler.

$$I_{Lo1,RMS} = I_{Lo2,RMS} = \frac{I_o}{2} \tag{17}$$

Shim inductance is another important component to extend the ZVS range, on the other hand, inductance value directly effects on the duty cycle loss interval. $C_{pri\text{-}coss}$ is primer switches output capacitance. According to the calculation in Eq. 18 [12], the shim inductance value L_{shim} is selected as 1.5 µH.

$$L_{shim} \geq 2 \cdot C_{pri\text{-}coss} \cdot \frac{V_{in}^2}{\left(\frac{I_{TR\text{-}pp}}{2} - \frac{\Delta I_{Lo1}}{2 \cdot \frac{N_p}{N_s}}\right)^2} \tag{18}$$

3.5. Calculations Related with Capacitors

Calculation of both output and input DC-link capacitor is given in this section.

Output load current ripple ΔI_o before DC-link capacitor is calculated as in Eq. 19, then RMS current value of output DC-Link capacitor $I_{Co\text{-}rms}$ which is critical to decide the number of paralleled capacitors is obtained. The amount of output voltage ripple ΔV_o decided as 2% of output voltage. As a result of calculation Eq. 21, the total output capacitance value C_o is selected as 90 µF. This capacitance value is achieved with paralleled nine pieces 10 µF capacitors which are MCJCU32MLB7106KPPDT1 from Taiyo Yuden.

$$\Delta I_o = 2 \cdot \frac{V_o \cdot (0.5 - D_{eff}) \cdot 10^{-5}}{L_{o1}} \tag{19}$$

$$I_{Co\text{-}rms} = \sqrt{\frac{1}{12} \cdot \Delta I_o^2} \tag{20}$$

$$C_o = \frac{V_o \cdot (1 - 2 \cdot D_{eff}) \cdot T^2}{16 \cdot L_{o1} \cdot \Delta V_o} \tag{21}$$

Input capacitance C_{in} is selected pursuant to the decided minimum input voltage V_{drop} that the converter could operate during the holdup time t_{hold} as in Eq. 22. C_{in} is selected as 6.6 µF when V_{drop} is 220 V and t_{hold} is 10 µs. The number of paralleled capacitors is determined according to the RMS current delivered from the C_{in} that is mentioned as $I_{Cin\text{-}rms}$ by Eq. 23 [10]. Two paralleled 3.3 µF capacitors are selected which are B32774P7335K from TDK Electronics.

$$C_{in} \geq \frac{2 \cdot P_o \cdot t_{hold}}{(V_{in}^2 - V_{drop}^2)} \tag{22}$$

$$I_{Cin\text{-}rms} = \sqrt{2 \cdot D_{eff}\left(\frac{I_o}{2} \cdot \frac{N_{sec}}{N_{pri}} - \frac{P_o}{V_{in}}\right)^2 + 2 \cdot (0.5\text{-}D_{eff})\left(\frac{P_o}{V_{in}}\right)^2} \tag{23}$$

3.6. Calculations Related with ZVS Condition

ZVS operation is considerably important in many aspects. PSFB converter has limitation to achieve ZVS since insufficient energy until reach the suitable operating condition. This situation is solved by using a clamping diode and shim inductor in this study. Eq. 24 has to be verified to achieve the ZVS condition.

$$Inductive\ Energy\ E_L \geq Capacitive\ Energy\ E_C \tag{24}$$

Inductive energy depends on the switching legs which are lagging and leading. Their inductive energy is calculated as in Eq. 25-26 respectively. S_1 and S_2 which are lagging leg switches, S_3 and S_4 which are leading leg switches. Capacitive energy is calculated by Eq. 27.

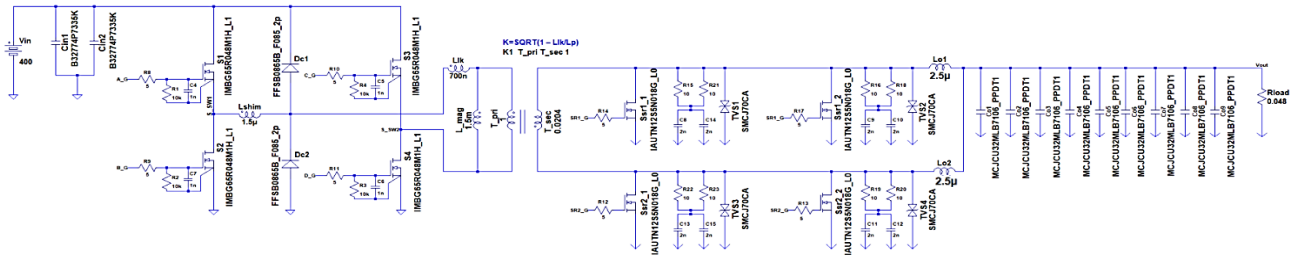

Fig. 3. PSFB with CDR converter simulation model in LTspice

C_{TR} could be neglected because of the explained reason in section 3.3. $C_{pri\text{-}coss(er)}$ is energy related output capacitance of primer switches. Circulating current over clamping diode on lagging leg switches has to be considered. $I_{clampd,min}$ and $I_{clampd,max}$ are the minimum and maximum current of the clamping diode during the freewheeling period correspondingly. $I_{mag,peak}$ is the maximum magnetizing current. $I_{Lo1,min}$ and $I_{Lo1,max}$ are the min. and max. current of the output inductor respectively.

$$E_{L\text{-}lagging} = 0.5 \cdot L_{lk} \cdot \left(I_{mag,pk} + I_{Lo1,min} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 + 0.5 \cdot L_{shim} \cdot \left(I_{clampd,\,min} + I_{mag,pk} + I_{Lo1,min} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 \quad (25)$$

$$E_{L\text{-}leading} = 0.5 \cdot L_{mag} \cdot I_{mag,pk}^2 + 0.5 \cdot L_{o1} \cdot \left(\frac{N_{pri}}{N_{sec}} \right)^2 \cdot \left(I_{Lo1,max} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 + 0.5 \cdot L_{lk} \cdot \left(I_{mag,pk} + I_{Lo1,max} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 + 0.5 \cdot L_{shim} \cdot \left(I_{clampd,\,max} + I_{mag,pk} + I_{Lo1,max} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 \quad (26)$$

$$E_c = 0.5 \cdot (2 \cdot C_{pri\text{-}coss(er)} + C_{TR}) \cdot V_{in}^2 \quad (27)$$

4. Simulation Results of the PSFB with CDR Converter

PSFB with CDR converter is simulated by using LTspice. Spice models of all selected components regarding to calculation are implemented. Simulation is done under the following operating conditions; 400 V input voltage, 12 V output voltage and 250 A output current. Simulation in LTspice is implemented as in Fig. 3. Efficiency is calculated as 95.7% for the simulated operating point. PWM waveforms which are belong to primary and secondary side switches are shared in Fig. 4. Phase shift is implemented according to the calculated duty cycle. Transformer voltage and current waveforms for both the primary and secondary sides are given in Fig. 5.

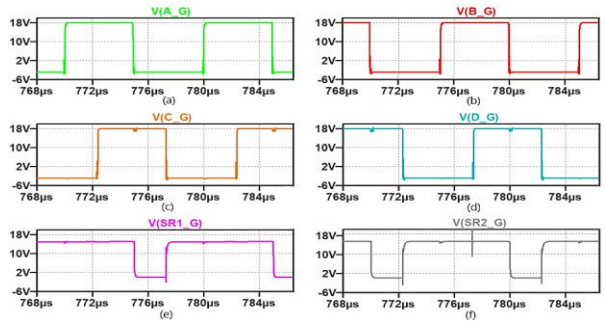

Fig. 4. Gate signals waveforms (a) of S1, (b) of S2, (c) of S3, (d) of S4, (e) of SR1, (f) of SR2

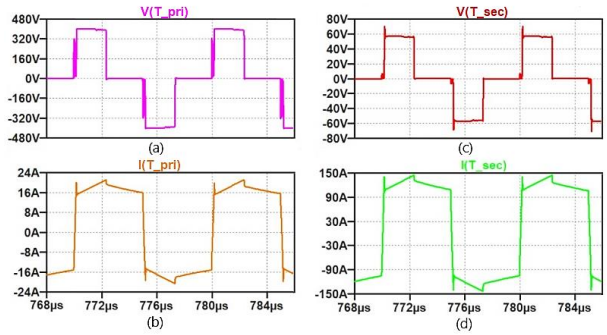

Fig. 5. Voltage waveforms (a) primary side and (c) secondary side of transformer; current waveforms (b) primary side and (d) secondary side of transformer

The waveform of output voltage which is 12 V, output current which is 250 A and output inductors current are given in Fig. 6.

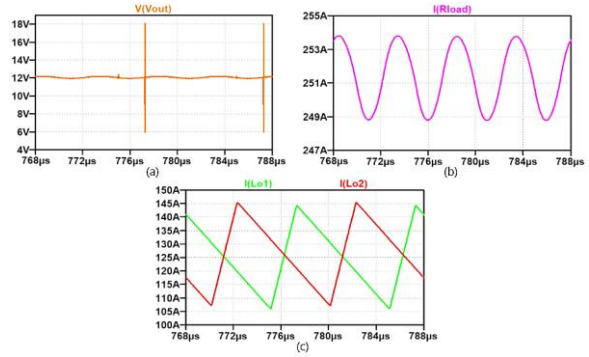

Fig. 6. (a) Output voltage waveform, (b) output current waveform, (c) output inductors (L_{o1} and L_{o2}) current waveform

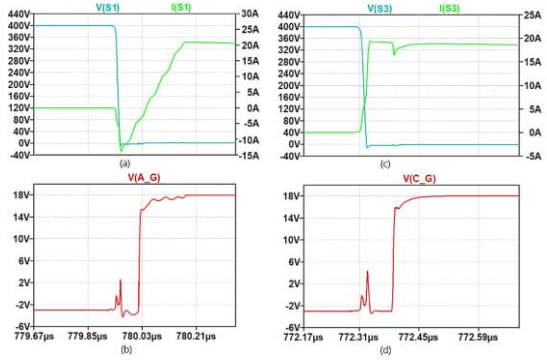

Fig. 7. (a) ZVS of S1 and (b) its gate signal waveforms; (c) ZVS of S3 and (d) its gate signal waveforms

ZVS operation for the lagging leg switch which is S1 and the leading leg switch which is S3 could be observed with consideration of PWMs which are belong to these switches during ZVS in Fig. 7. With the help of this feature, high efficiency is obtained.

5. Prototype and Experimental Results of the PSFB with CDR Converter

PSFB with CDR is implemented as PCB with selected components according to calculations in section 3. PCB designed as multi-layer. Power density is 1.87 kW/L. The designed and implemented prototype PCB as first prototype is given in Fig. 8.

Input and output voltage and current waveforms could be observed at operating condition which is 400 V input voltage, 12 V output voltage, and 250 A output current in Fig. 9.

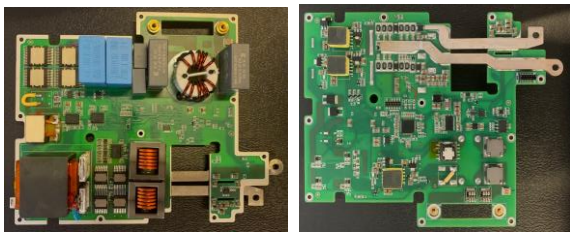

Fig. 8. Top view at left and bottom view at right of implemented PSFB with CDR converter

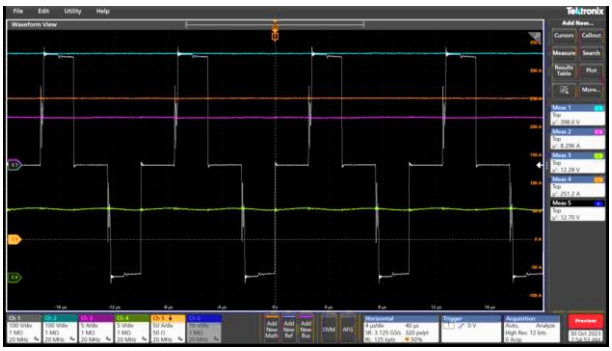

Fig. 9. Input voltage (blue), output voltage (green), input current (pink), output current (orange)

Efficiency is measured as 93.4% from implemented design. There is efficiency difference between simulation and experimental results. There might be several reasons which cause this variance. The most dominant one is power loss in PCB trace since output current is considerably high. Improvements on conduction losses are evaluated for the next prototype to reach the higher efficiency as obtained in simulation.

6. Conclusions and Future Works

In this paper, design calculations, and component selections of 3 kW PSFB with CDR topology as APM of EV are completed for varying input voltage between 240 V and 475 V, the output voltage between 10.9 V and 14 V. Simulation with spice model of components is realized under the operating condition of 400 V input voltage, 12 V output voltage, and 3 kW output power. For this operation, efficiency is calculated as 95.7% from the simulation. The converter is implemented and tested under the same operating condition and efficiency is measured as 93.4% with 1.87 kW/L power density. Power density is high when similar designs which have microcontroller, gate drivers, magnetics, switches and input filter stage at the same PCB, are considered. High compatibility between calculated values and both simulation and experimental results are obtained however the efficiency of the experimental result is lower than the simulation result. ZVS loss during light load operation for lagging lag and voltage overshoot phenomena at primary switches are solved with the usage of clamping diodes.

As a future work, efficiency improvement for the implemented design will be evaluated and applied to the next prototyped PCB.

7. References

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