Implementation of DAB Converter with DC Blocking Capacitors and Multiple Switch Fault Tolerant Capability with Proposed SPSFT Controller

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***Abstract*—In this study, Modified Dual Active Bridge (DAB) converter with DC blocking capacitors and multiple Switch Fault-Tolerant (FT) Capability with Proposed Single Phase-Shift FT (SPSFT) Controller is proposed due to the high efficiency and robustness in the different applications. The Switch FT converters are mostly focused on Open-Circuit Fault (OCF) and generally only one fault per circuit. However, Short-Circuit Fault (SCF) is also critical concerns for power converters, and it is usually more dangerous especially with battery connected applications due to risk of over discharging. Moreover, converters generally face more than one switch fault during the lifecycle. However, the current approaches cannot solve directly these problems by handling both SCF and OCF errors and multiple fault tolerance. DC blocking capacitors ensure safety in the SCF states and prevents inevitable short-circuit paths in both Primary and Secondary Side of the circuit. Controller detects faulty switches with voltage and current measurements and selects the suitable switching pattern in post fault states without interrupting the output power flow. Analysis of the nominal and post-fault conditions are given in detail up to the three switch faults. Finally, MATLAB-Simulink simulation results are given in this paper to verify the robustness and stability of the proposed circuit and controller.**

Keywords— Fault-Tolerant (FT), Open-Circuit Fault (OCF), Short-Circuit Fault (SCF), Dual Active Bridge (DAB) Converter, Single Phase Shift Fault Tolerant (SPSFT) Controller

I. INTRODUCTION

The popularity of fault-tolerant converters is scaling up in both research in the academic papers and industrial applications due to increasing needs for continuous power supply feature for the security in the critical applications such as medical, defense industry, electrical vehicles and space applications even after switch faults [1]. In these applications, interrupted power flow even in fault situations is very crucial. Nowadays' research interest in both academic papers and industrial projects focused on fault-tolerant converters in both DC-DC [2] and AC-DC Converters [3].

In critical applications like EV, continuous power flow and fault handling is very crucial because it can cause control failures and even in SCF states, it can provoke battery damages, [4]. In the literature, fault-tolerant converters are proposed on different topologies with different ways. Generally, DC-DC converters take more attention because most of the electronic systems works with DC electricity. For fault tolerance, generally there are two approach in the converters. Module based redundancy and switch based redundancy. Module based redundancy uses same circuit twice or more. This can ensure power flow but it also increase the price and volume of the power systems drastically [5]. On the other hand, switch based redundancy is a rising trend in the power electronics fields. It can ensure power flow without increasing price and volume excessively [6].

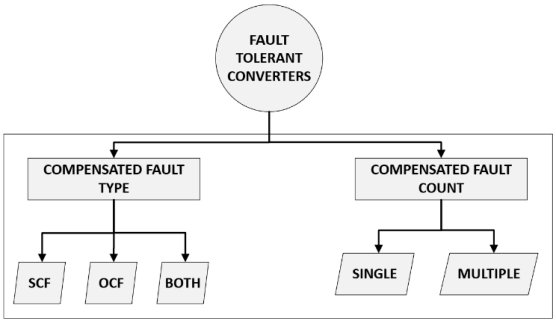


Fig. 1. General Fault-Tolerant Converter Types based on Handled Fault Types and Fault Count.

In the literature, papers and applications for switch redundancy mostly focused on handling only one OCF errors [7]. However in the power converters, SCF is also a common fault state and it is more dangerous than OCF because it cause over-current on faulty legs of the converters [8]. It can cause over-discharging on the batteries and can damage whole system [9]. General structure of the types of the FT Converters are shown in Fig. 1.

In [10], three phase Fault Tolerant (FT) Dual Active Bridge (DAB) converter is proposed. It can handle two OCF errors but it cannot handle SCF errors. In [11], FT circuit for a DAB converter is proposed for both handling SCF and OCF errors but it can only handle one fault. In [12], multiple OCF tolerant modified DAB converter is proposed. It uses divided input and output capacitances and center tapped transformer to handle faults. In [13], the fault tolerant LLC circuit is proposed. It can handle up to two SCF and OCF errors but, it is limited only Primary Side of the circuit. Secondary is made up with diodes so this work cannot have tolerance on Secondary Side failures. To ensure multiple SCF and OCF faults in both primary and Secondary Side of the circuit, the DAB circuit with DC blocking capacitors and SPSFT controller is proposed based on [13] and DAB converter. Proposed circuit can handle both SCF and OCF errors up to the three faults for all circuit and two faults for individual primary or Secondary Side.

In section 2, the steady-state operation of the converter is explained. In section 3, fault detection is explained. In section 4, SPSFT controller is explained. In section 5, post fault

operation modes of the converter are explained. In section 6, MATLAB-Simulink simulation circuit and results are given. Finally, conclusion part is given in this paper.

II. PROPOSED FAULT TOLERANT DAB CONVERTER

A. General Structure of the Proposed Circuit

The DAB converter circuit structure is shown in Fig. 2. DAB Converter is selected for FT application in proposed circuit due to wide load and input range high efficiency with Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) features, robust control structure, different control options like Phase Shift Modulation (PSM) and Frequency Modulation (FM) [14], [15], [16].

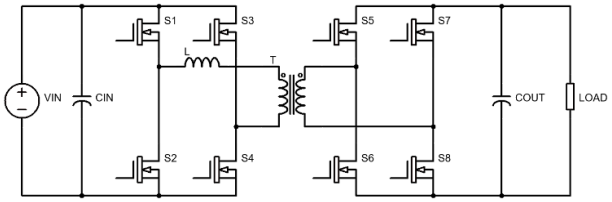


Fig. 2. Circuit Structure of DAB Converter.

The proposed FT-DAB converter circuit has fundamental parts of primary bridge legs, secondary bridge legs, two high frequency isolation transformers, auxiliary inductors and DC blocking capacitors. It is shown in Fig. 3. The proposed SPSFT controller is used to control output voltage in the proposed circuit so auxiliary inductors are used to ensure stable power flow between primary and secondary bridges. Inductors can also provide a wide range of ZVS and ZCS for the MOSFETs in suitable control situations. Three Half-Bridge legs in both primary and secondary are used to handle different fault scenarios in the converter. In different fault situations, switches and transformer branches that are used can change. HF transformers are used to ensure galvanic isolation between input and output and increase safety of the DC-DC Converter. Transformers are connected series in both primary and secondary to handle all types of errors like SCF and OCF and give voltage doubling in secondary in most of the operation modes. This provides benefits such as lowering current and voltage stress on the switches and transformers and more robust control. DC blocking capacitors are used to ensure to block short-circuit paths when SCF faults occur [17]. They also reset DC voltage offsets on the HF transformers [18], [19].

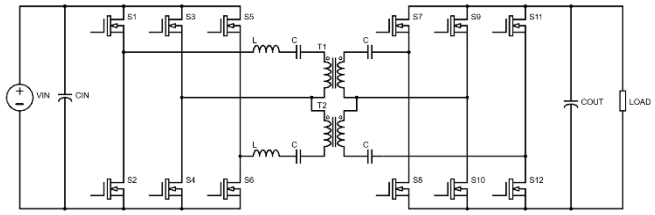


Fig. 3. Circuit Structure of Proposed FT-DAB Converter.

B. Steady State Operation Mode

The first operation mode of proposed circuit is nominal operation condition. It is called Mode 1 in this paper. In Mode 1, both in primary and secondary, switches work in full bridge formation with defined phase-shift. In primary, Switches S1-S6 and S2-S5 turn on and off together in duty ratio of 50% in ideal. In real applications like simulation and real circuit, the dead time is needed to ensure proper turn on and off cycles of the switches and ZVS features. There is a constant 180º phase shift between S1 and S5 switches. In Secondary Side, S7-S12 and S8-S11 turn on and off together and there is also a constant 180º phase-shift between S7 and S11. Due to SPS modulation in the control system, there is a defined Phase Shift (PS) *Q* between S1 and S7 in order to control output voltage. PS ratio is defined by SPSFT controller based on output voltage error. The details of the controller are given in Section 4. The switching pattern in the Mode 1 is shown in Fig. 4.

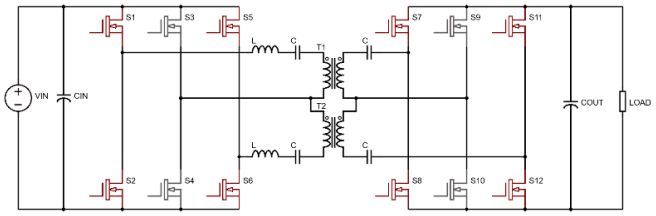


Fig. 4. Proposed Converter in Mode 1.

In Mode 1, both transformers simultaneously transfer power to the secondary side. Owing to the polarity configuration of the transformers, the secondary-side voltage is effectively doubled, thereby reducing the required phase-shift ratio compared to the other operating modes. Moreover, since current is distributed between the two transformers, the current stress on each unit is significantly reduced relative to the modes utilizing a single transformer. Under normal operating conditions, the converter functions in Mode 1 until the first fault event occurs.

In the mode diagrams, the colors of the switches indicate their respective operating states: dark red represents nominal operation, bright red indicates a short-circuit condition, gray denotes an open-circuit condition, and black corresponds to an unused but undamaged state.

III. FAULTY SWITCH DETECTION

Fault detection is the first step in the system for continuous power flow. SCF and OCF faults affect switching node voltages and line current differently according to position of switch and type of fault [20].

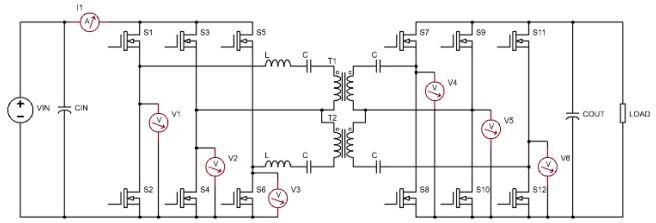


Fig. 5. Fault Detection of Converter with the Voltage/Current Measurement.

In order to measure the line current and switching node voltages, 6 voltage and 1 current sensor are added to the circuit's Primary and Secondary Sides. With these measurements, SPSFT controller can decide which switch has an error and its type, then can change the working mode of the converter. Position of the voltage and current sensors is shown in Fig. 5.

If the SCF error happens in any switch, dI/dt (slope) of the line current increases. Moreover, if the error happens in the upper switches, dV/dt of the voltage rises on switching node; but if it happens in the lower switches, dV/dt of the voltage drops on that node. However, for OCF errors, it is vice versa. Detailed behavior of the switches in the different fault situations is given in Table I.

After the Second Fault, the matrix of possible switches gets very complex so in the table, possible switches in Mode 3 are shown as SX and SY as a bridge leg switch pairs and VX is their switching node.

TABLE I. FAULT DETECTION OF SWITCHES

Fault Detection Mode	SCF and OCF Behavior of the Measuring Points		
	Switch	*SCF*	*OCF*
		Input current increase drastically	-
MODE 1	S1	V1 increases	V1 decreases
	S2	V1 decreases	V1 increases
	S5	V3 increases	V3 decreases
	S6	V3 decreases	V3 increases
	S7	V4 increases	V4 decreases
	S8	V4 decreases	V4 increases
	S11	V6 increases	V6 decreases
	S12	V6 decreases	V6 increases
MODE 2	S3	V2 increases	V2 decreases
	S4	V2 decreases	V2 increases
	S9	V5 increases	V5 decreases
	S10	V5 decreases	V5 increases
MODE 3	SX	VX increases	VX decreases
	SY	VX decreases	VX increases
MODE 4	-	-	-

IV. SPSFT CONTROLLER

A. Single Phase Shift Modulation

In this paper, Single Phase Shift Modulation is used to control output voltage of the DAB converter. SPS is used because it is simple, efficient and usable in fault conditions [21], [22]. Control diagram of SPS controller is shown in Fig. 6. SPS controller uses voltage error and PI controller to detect proper phase-shift Q. From that phase shift time T1 is calculated with a switching period. Its formula is given in (1).

$$T1 = \frac{Q}{360} \cdot T_s \tag{1}$$

After the calculation, time shift is applied on gate signal of primary reference switching signal and time shifted signal applied secondary reference switch. S1 is the primary reference switch, it has no time shift, S7 is the secondary reference switch. It has variable phase-shift Q that can vary between [0º - 90º]. The remaining switch pairs in both primary and secondary have constant 180º phase-shift to prevent short circuits.

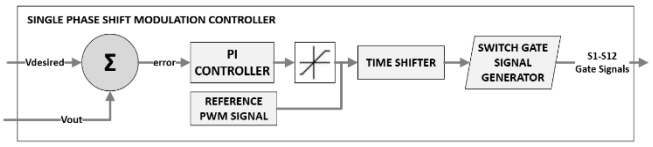


Fig. 6. SPS Gate Signal Generation Diagram.

B. Fault Tolerant Controller

Fault tolerant controller uses voltage and current measurements to determine faulty switch with based on voltage and current changes given on Table I. Nominal levels of the switching node voltages and line current in different modes obtained by simulations. In the controller there are four signal assignments for the switches. PWM1, PWM2, 0 and 1. PWM1 and PWM2 are used for switching that are given by SPS modulation. 0 and 1 are used to control switches in cut-off and conduction modes. General controller diagram is shown in Fig. 7. There is a waiting time for control system after every fault to ensure get steady state values of all measured voltages and current. Waiting time is crucial for system. If it is not used in the system, that can cause critical errors in detection process of faulty switches and fault types.

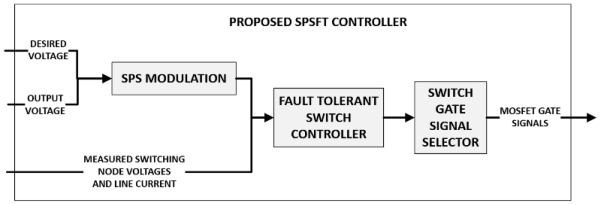


Fig. 7. General SPSFT Controller Diagram.

There is a large fault tolerance matrix due to switch count but in this paper all three fault modes is presented with selected three switches. Switch SCF error diagram is shown in Fig. 8. It shows switches that can cause SCF or OCF errors in different working modes.

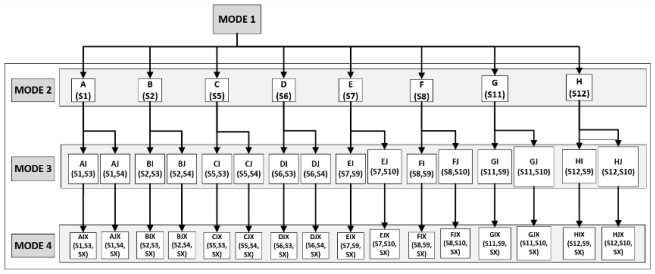


Fig. 8. SCF Error Flow Diagram.

V. POST FAULT OPERATION MODES

After the detection of the faulty switch, controller changes the working mode according to the faulty switch and fault type and converter works with new switching pattern to continue power flow to the load. In this paper, switches S2, S3 and S12 are selected with SCF fault for analysis of the post-fault working modes. SCF fault is selected because it is more dangerous and difficult to handle than OCF errors in the power converter. In addition, the handling steps for both SCF and OCF errors are very similar.

A. Mode 2

When the first SCF fault happens in the switch S2; in order to protect converter from over-currents and continue to the power flow, controller makes S1, S6, S7 and S11 switches open circuit and S5,S8 and S12 switches short circuit. Switching continues on the S3-S4 switches. In Mode 2, both HF transformers are used to transfer power but due to the change of the voltage polarities, it loses the voltage doubling feature on the Secondary Side. To compensate that difference, SPS controller increase phase-shift ratio to maintain output voltage. The switching pattern in the Mode 2 is shown in Fig. 9.

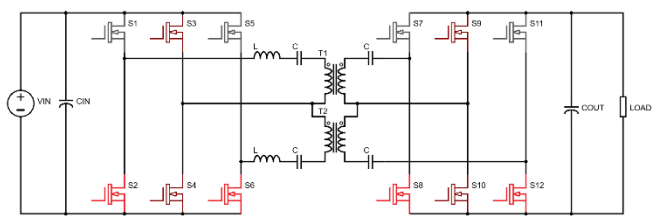


Fig. 9. Proposed Converter in Mode 2.

Due to polarity effect of the changing Primary Side pattern on the Secondary Side, Secondary Side switching pattern also changed. Primary and Secondary Side have same switching patterns. However in the Secondary Side faults, it is not necessary to change switching pattern of the Primary Side because Primary Side is not dependent on Secondary Side in source to load power flow. It can give more effective switching patterns, if the Primary Side manipulations are considered but, it is not examined in this paper.

B. Mode 3

After the first fault in the S2, there are possible two switches for second fault in the Primary Side. They are S3 and S4. If second SCF fault happens in the S3 switch, controller shifts system to the Mode 3 so as to continue power flow. In Mode 3, due to SCF error in S3, controller switch S4 and S10 MOSFETs to the cut-off mode and switching continues on S5 and S6 switches. The switching pattern in Mode 3 is shown in Fig. 10.

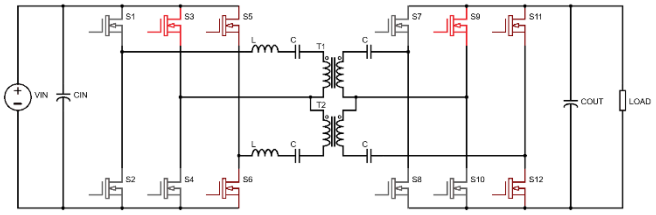


Fig. 10. Proposed Converter in Mode 3.

Due to Half-Bridge switching pattern in Mode 3, only second HF transformer is used to flow power and increase current stress on the transformer but controller ensures to constant output voltage with adapting suitable phase-shift.

C. Mode 4

When the third fault happens on the S12 switch in the Secondary Side, the controller switches system to Mode 4. The controller changes the switching pattern to handle Secondary Side fault also. Because of the SCF on S12, controller makes S11 switch open circuit and switching continues on Secondary Side with S9 and S10 switches. The switching pattern in Mode 4 is shown in Fig. 11.

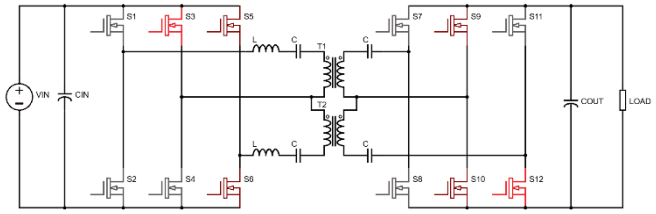


Fig. 11. Proposed Converter in Mode 4.

Due to previous errors, only the second HF transformer delivers power in Mode 4 also. The order of switch fault can change like Primary → Primary → Secondary (PPS), Primary → Secondary → Primary (PSP) etc. Due to large error possibility, the total error matrix is very large but with predefined switching patterns, system can handle most of the possible fault orders in lifecycle. However, if all three faults happen on the Primary Side or Secondary Side (PPP or SSS), the system cannot handle those patterns because there is no suitable path for switching after three faults on same side. In this paper, the fault order is PPS. Fault order map is given in Fig. 12.

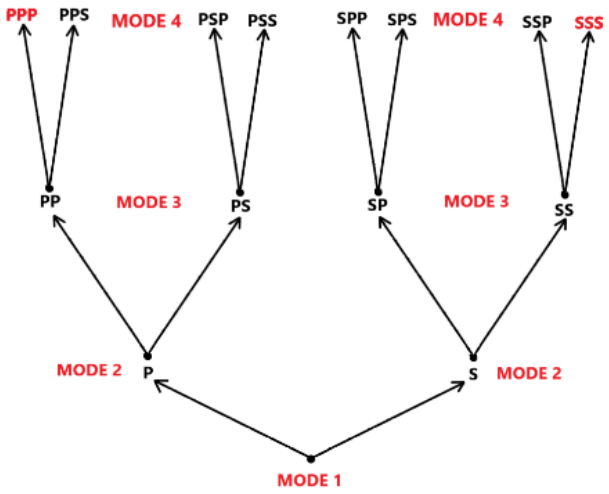


Fig. 12. Switch Fault Map of the Converter.

VI. MATLAB-SIMULINK SIMULATION

To verify the fault tolerant feature and proposed SPSFT controller, SIMULINK simulation is performed. Three different working modes are shown to observe behavior of the system in post-fault conditions.

A. DC Blocking Capacitors Calculation

DC blocking capacitor is the important part of the converter. If value of the capacitor isn't selected properly, it can cause resonance and it changes system behavior and dynamics completely. To prevent that case, the capacitance value should be selected considering the system properties such as switching frequency. Calculation formula is given in (2).

$$C_{dcb} = \frac{100}{4 \cdot \pi^2 \cdot f_s^2 \cdot L_{aux}} \tag{2}$$

With given formula, needed minimum blocking capacitor value is calculated. Moreover in the proposed circuit, Mode 1 and Mode 2 uses both HF transformer so it makes 2 blocking capacitance as a series connected. Due to that, $2 \cdot C_{dcb}$ value is used to prevent oscillations in every mode of the system.

Proposed circuit is implemented in the SIMULINK to verify the system. DAB converter properties that are used in the simulation are given in Table II.

TABLE II. DAB CONVERTER PROPERTIES

Parameter Table	**Simulation System Parameters**		
	Parameter Table	***Abbreviation***	***Value***
Parameters, Values and Abbreviations	Input Voltage	V_{in}	120 V
	Output Voltage	V_{out}	80 V
	Output Power	P_{out}	300 W
	Switching Frequency	f_s	20 kHz
	Auxiliary Inductance	L_{aux}	35 µH
	Magnetizing Inductance	L_{mag}	300 µH
	Transformer Turn Ratio	n	1:1
	DC Blocking Capacitor	C_{dcb}	250 µF

B. Simulation Circuit

In order to verify proposed system, MATLAB-SIMULINK software is used to implement proposed converter and controller. Simulation circuit has five main parts. Modified DAB converter, SPS modulator, FT controller, Switch Input Selector (SIS) and observation scopes. Simulation circuit is shown in Fig. 13.

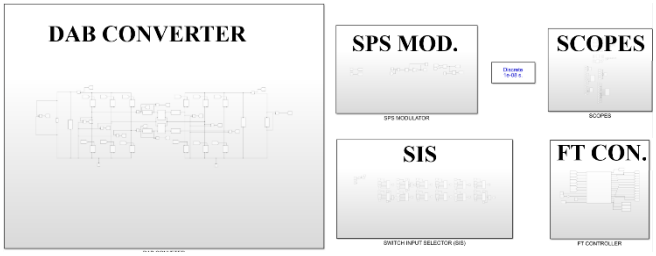


Fig. 13. Simulation Circuit of the Proposed Converter.

Four different operating modes are tested in the simulation, and the output voltage, power, efficiency, and corresponding waveforms are observed for each mode to verify the theoretical expectations and fault-tolerant capability of the converter. For the fault analysis, switches S2, S3, and S12, as well as the short-circuit fault (SCF) condition, are selected.

C. Simulation Results

Mode 1 is observed firstly in the simulation, it gives 80V steady output voltage without any big fluctuation and instability in controller and DAB waveforms. Overall efficiency in Mode 1 is approximately 97% in the simulation. Mode 1 waveforms are shown in Fig. 14.

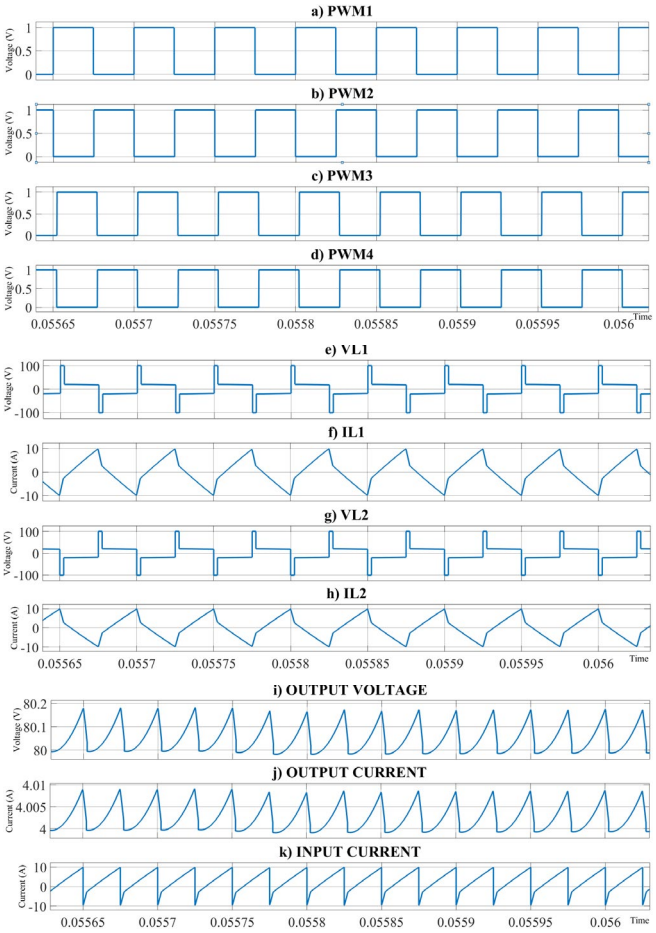


Fig. 14. Waveforms in Mode 1. **a)** PWM1, **b)** PWM2, **c)** PWM3, **d)** PWM4, **e)** V_{L_aux1}, **f)** I_{L_aux1}, **g)** V_{L_aux2}, **h)** I_{L_aux2}, **i)** Vout, **j)** Iout, **k)** Iin.

In Fig. 14, generated PWM pulses are shown in a, b, c and d. Output voltage is shown in i. Output current is shown in j. Input current is shown in k. Voltage and current on first auxiliary inductor are shown in e and f. Voltage and current on second auxiliary inductor are shown in g and h.

After the first SCF in S2 switch at 0.1 second in simulation, system switch to Mode 2. Switching pattern and phase-shift are changed so waveforms are effected. Due to new modified switching path, efficiency is drops to the approximately 94%. Mode 2 waveforms are shown in Fig. 15.

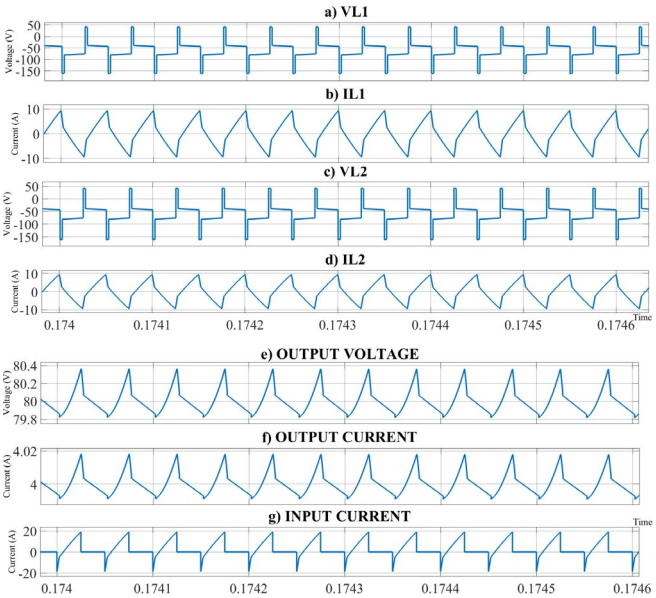
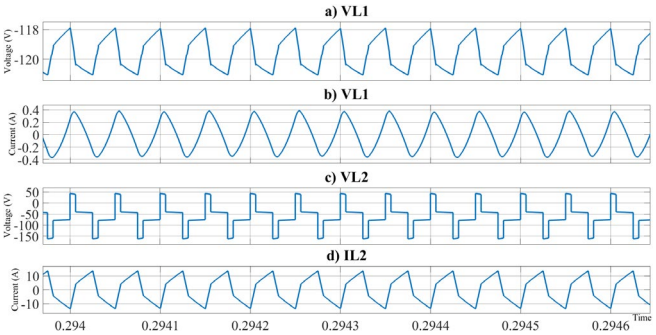


Fig. 15. Waveforms in Mode 2. **a)** V_{L_aux1}, **b)** I_{L_aux1}, **c)** V_{L_aux2}, **d)** I_{L_aux2}, **e)** Vout, **f)** Iout, **g)** Iin.

In Fig. 15, output voltage is shown in e. Output current is shown in f. Input current is shown in g. Voltage and current on first auxiliary inductor are shown in a and b. Voltage and current on second auxiliary inductor are shown in c and d.

After the second SCF in S3 switch at 0.2 second in simulation, system switch to Mode 3. Second fault also has impacts on systems due to new switching sequence. Due to changes in switching sequence, overall efficiency is approximately 93%. Mode 3 waveforms is shown in Fig. 16.



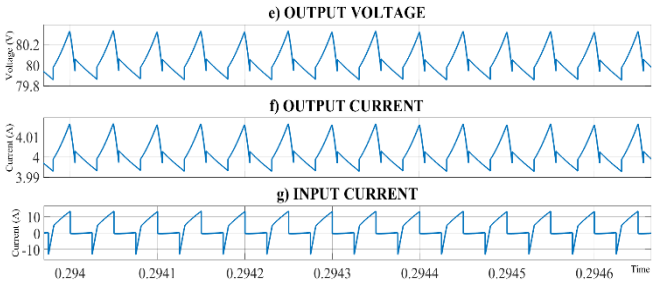


Fig. 16. Waveforms in Mode 3. **a)** V_{L_aux1}, **b)** I_{L_aux1}, **c)** V_{L_aux2}, **d)** I_{L_aux2}, **e)** Vout, **f)** Iout, **g)** Iin.

In Fig. 16, output voltage is shown in e. Output current is shown in f. Input current is shown in g. Voltage and current on first auxiliary inductor are shown in a and b. Voltage and current on second auxiliary inductor are shown in c and d.

When third SCF happens at 0.3 second in S12, systems switches Mode 4. Secondary switching cycle changes to handle last error. After that, system works under S2, S3 and S12 SCF condition with only losses 4% of the efficiency. In Mode 4, overall efficiency is approximately 93% also. Mode 4 waveforms is shown in Fig. 17.

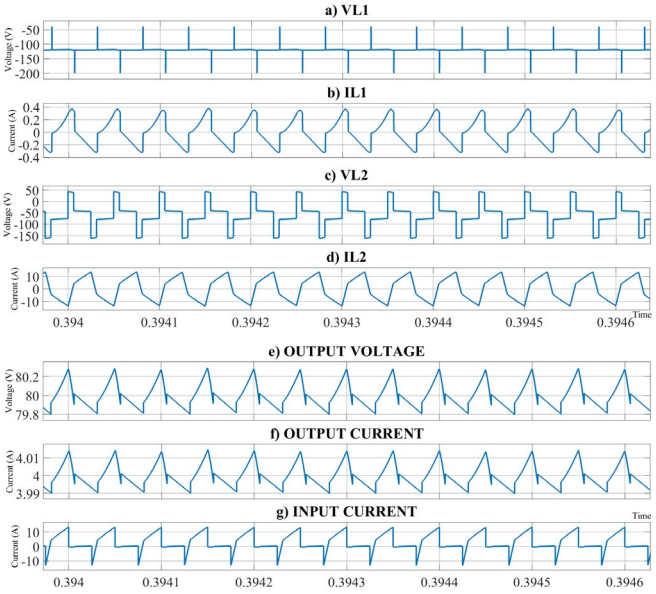


Fig. 17. Waveforms in Mode 4. **a)** V_{L_aux1}, **b)** I_{L_aux1}, **c)** V_{L_aux2}, **d)** I_{L_aux2}, **e)** Vout, **f)** Iout, **g)** Iin.

In Fig. 17, output voltage is shown in d. Output current is shown in e. Input current is shown in f. Voltage and current on first auxiliary inductor are shown in a and b. Voltage and current on second auxiliary inductor are shown in c and d.

The overall system response to the faults are swift to prevent power losses on the output but there is slight fluctuation on the output voltage during first times after faults but fluctuations can be improved with further studies on the fault detection algorithm. The overall system waveforms during whole simulation are shown in Fig. 18.

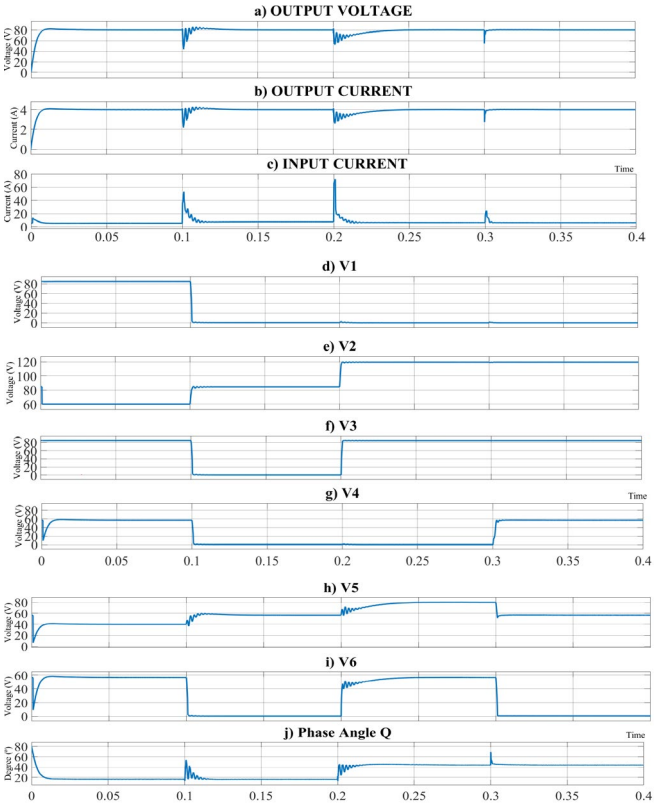


Fig. 18. General System Waveforms in All Modes. **a)** Vout, **b)** Iout, **c)** Iin (RMS), **d)** V1, **e)** V2, **f)** V3, **g)** V4), **h)** V5, **i)** V6, **j)** Phase-Shift Angle (Q).

In Fig. 18, output voltage is shown in a. Output current is shown in b. RMS input current is shown in c. Switching node voltages that are using for fault detections are shown in d, e, f, g, h and i. Phase-shift angle of the SPS modulator is shown in j.

The simulation results verifies theorical expectations. Proposed converter and controller can handle three SCF errors and deliver interrupted power to the output with over 93% efficiency and without any oscillation and instability. Waveforms changed between modes due to DAB structure changes along the modes. In first mode, system work as a DAB converter but in other modes, it works as a Dual Active Half Bridge converter. This effects needed phase-shift ratio and efficiency also. However, SPSFT controller compensate this difference and stabilize output voltage even in the fault conditions.

CONCLUSION

In In this study, a Multiple Short-Circuit Fault (SCF) and Open-Circuit Fault (OCF) tolerant Dual Active Bridge (DAB) converter with a Single Phase-Shift Fault-Tolerant (SPSFT) control strategy has been proposed. The operating principles of the converter in Mode 1 and Modes 2–4, together with the corresponding fault detection parameters, have been thoroughly analyzed. Simulation studies have been performed in MATLAB/Simulink to validate the proposed system's robustness, stability, and fault-tolerant capability. The results demonstrate that the proposed strategy can sustain up to three simultaneous switch open-circuit or short-circuit faults without interruption of output power, while maintaining efficiency with only a 4% reduction even under triple-fault conditions. The robustness of the proposed control method has been further verified through switching waveform analysis.

Overall, the findings confirm the effectiveness of the proposed SPSFT-controlled DAB converter for fault-tolerant power conversion. Future work will focus on extending the system by integrating advanced modulation techniques such as Extended Phase Shift (EPS) and Resonant DAB (CLLC) operation, as well as implementing improved fault detection algorithms to enhance efficiency and reliability.

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