Fully Active Meminductor Emulator Circuit

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Abstract

This work introduces an active-only architecture for a meminductor emulator, where the required capacitive behavior is derived solely from the inherent gate capacitances of MOS devices, removing the need for any external capacitors. By avoiding passive elements, the proposed approach notably decreases the silicon area demanded in IC implementations. Validation through Cadence-based simulations using a 0.18 µm CMOS process demonstrates that the practical behavior of the circuit aligns well with the theoretical model and confirms its viability.

Keywords: Active meminductor architecture, Memory characteristics, Intrinsic-capacitance-based design

1. Introduction

The memristor—identified by Leon Chua as a passive device connecting flux and charge—was first introduced in the early 1970s [1]. After the memristor gained substantial attention and demonstrated its conceptual power, the idea of memory-enabled circuit elements was broadened to include capacitive and inductive variants as well [2]. Much like memristors, memcapacitive and meminductive devices show history-dependent behavior, typically visualized through a pinched hysteresis loop relating their internal state variables. Beyond this, they are capable of storing energy either electrostatically or magnetically, making them appealing candidates for neuromorphic and bio-inspired electronic systems [3]. Since these components can simultaneously hold and process information, they are expected to contribute to the realization of low-power, brain-inspired computational platforms [4]. Nevertheless, the absence of reliable solid-state realizations of memcapacitors and meminductors remains a major obstacle, leading researchers to focus on emulation circuits that reproduce their mathematical descriptions and dynamical properties.

A substantial body of work has explored meminductor emulation using various analog building blocks in combination with passive devices. Reported examples include mutator-based arrangements employing multiple current conveyors, buffers, multipliers, current sources, and external passive elements [5]. Other implementations—such as memristor-free current-driven designs—utilize several current conveyors, arithmetic circuits, and multiple passive components, with corresponding voltage-driven counterparts constructed from similar device sets [6]. Further published structures consist of MOSFET-only arrangements combined with multipliers and operational amplifiers, as well as circuits integrating buffers, multipliers, operational amplifiers, current conveyors, and numerous passive parts [7]. Designs based on gyrator principles have also been proposed, requiring operational amplifiers along with passive elements [8]. Additional variations feature compact arithmetic units with a small number of passive components [9], or more complex arrangements including numerous passive elements and several amplifiers [10]. Floating mutator approaches use operational amplifiers, current conveyors, varicap diodes, and passive components, while other solutions incorporate multipliers and current conveyors together with passive networks [11-12]. Hybrid systems combining operational amplifiers, current conveyors, multipliers, OTAs, and a considerable number of passive parts have likewise appeared in the literature [11]. Some configurations rely on combinations of multipliers, operational amplifiers, and current conveyors supported by passive networks [13]. A relatively minimalistic alternative employs a memristor together with operational amplifiers, a capacitor, and resistors [14].

Although diverse in structure, most of these emulators rely on traditional circuit-design methodologies, and consequently depend on external passive elements. Such dependence increases chip area and can negatively influence power efficiency, factors that are particularly problematic in integrated and low-power systems. Motivated by these constraints, the present work proposes a meminductor emulator circuit (MIC) that completely avoids the use of passive components. The emulator is built solely from active circuitry, and its behavior is benchmarked against previously published designs. Simulations based on the XFAB 0.18 µm CMOS technology were carried out, and an equivalent non-ideal model was introduced to investigate the influence of non-idealities on the emulator's performance.

The remainder of this paper is structured as follows: Section 2 outlines the conceptual basis and architecture of the proposed MIC. Section 3 presents the obtained simulation results. Non-ideal effects and their implications are discussed in Section 4. Section 5 offers a comparison with other representative designs in the literature. Finally, Section 6 summarizes the main conclusions and contributions of this study

2. Realization of Proposed MIC

A meminductor can be described through the fundamental linkage between charge and flux, forming the basis of its behavioral definition:

$$\varphi_L(t) = L_M[\int_{t_0}^{t} i(\tau)d\tau]i(t) = L_M(q)i(t). \qquad (1)$$

This expression represents a charge-driven meminductive element in which the flux (φ) evolves as the time integral of the applied voltage. The block-level layout of the designed MIC is shown in Fig. 1. In this structure, the emulator is formed solely using active building blocks, eliminating the need for discrete passive elements by exploiting the intrinsic capacitances of MOS transistors.

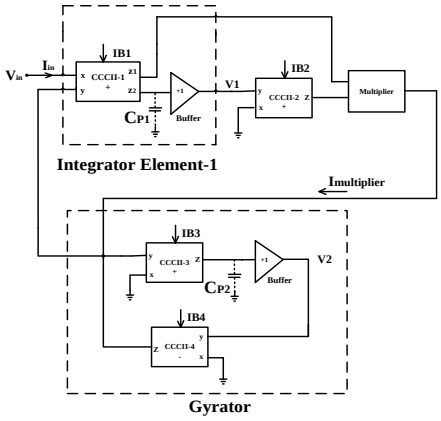


Fig. 1. Architecture of the proposed active-only meminductor emulator

By using the above formulation, the governing equations that describe the electrical characteristics of the developed emulator can be derived as follows:

$$V_1 = \frac{1}{C_{P1}} \int I_{in}(t)dt = \frac{q_{in}}{C_{P1}} \tag{2}$$

$$I_{z2} = g_{m2} V_1 = \frac{g_{m2}}{C_{P1}}\, q_{in} \tag{3}$$

The multiplier output:

$$I_{multiplier} = \frac{g_{m2}}{C_{P1}}\, \mathrm{q}_{in} \text{ x } I_{in} \tag{4}$$

A standard examination of the gyrator structure leads to the following set of relations:

$$V_2 = \frac{1}{C_{P2} r_{x3}} \int V_{in}(t)dt = \frac{g_{m3}}{C_{P2}}\, \varphi_{in} \tag{5}$$

$$I_{multiplier} = \frac{V_2}{r_{x4}} = \frac{g_{m3}}{r_{x4}\, C_{P2}}\, \varphi_{in} \tag{6}$$

Using the relation in (6) within the expression given in (4), the resulting formulation can be expressed as:

$$\frac{g_{m3}}{r_{x4}\, C_{P2}}\, \varphi_{in} = \frac{g_{m2}}{C_{P1}}\, q_{in}\, x\, I_{in} \tag{7}$$

$$L_M = \frac{\varphi_{in}}{I_{in}} = \frac{g_{m2}}{g_{m3}} \frac{C_{P2}}{C_{P1}}\, q_{in}\, r_{x4} \tag{8}$$

Fig. 2a illustrates the CCCII structure, which is implemented using a standard trans-linear configuration. The corresponding voltage buffer is shown in Fig.2b.

In this work, an alternative meminductor architecture is introduced, featuring a fully active structure that operates without any external passive elements. This approach substantially decreases the required silicon area. The capacitances essential for achieving the desired inductive behavior are derived directly from the natural gate capacitances of MOS transistors operating in saturation. By enlarging the gate dimensions of specific transistors, the impact of nonlinear junction capacitances is mitigated. Since MOS devices provide much higher capacitance density than standard metal–insulator–metal capacitors, they offer a compact solution for integrated circuit implementations [15].

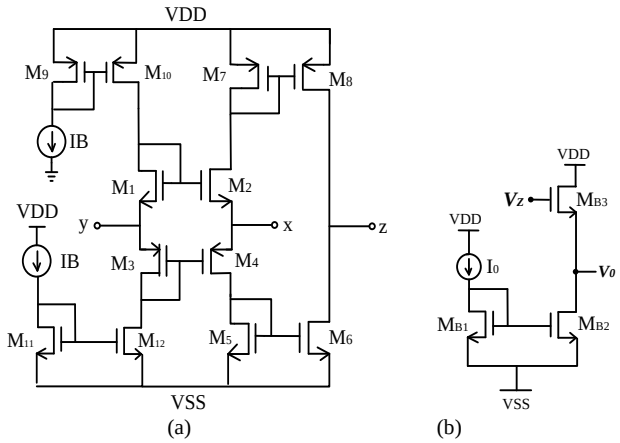


Fig. 2. (a) Trnasistor level diagram of the CCCII using CMOS technology, and (b) circuit diagram of the voltage-buffer stage.

In designing the circuit shown in Fig. 1, transistor geometries were selected with particular care: minimum-size devices were used within the CCCII structure to enhance bandwidth, while the MOSFETs connected to the buffer's input were intentionally made larger to increase the intrinsic capacitance at that node. The device dimensions used in both the CCCII and buffer stages are listed in Table 1.

Table 1. Device dimensions adopted for the CCCII block

Transistor	CCCII (W/L, μm)
M_1-M_2	5/0.8
M_3-M_4	12/0.8
M_5	3/0.8
M_6	6/0.8
M_7	1.5/0.8
M_8	4/0.8
M_9-M_{10}	4/0.8
M_{11}-M_{12}	2/0.8
M_{B3} (buffer)	35 /0.8
M_{B1}-M_{B2} (buffer)	2/0.8

2.1. Multiplier Sub-circuit

The multiplier block can be constructed using the mathematical relation provided in [16].

$$(X+Y)^2 - (X-Y)^2 = 4XY \tag{9}$$

In the configuration presented in Fig. 3, the circuit relies on two distinct translinear loops to execute the required nonlinear operations. The first loop, built around transistors M1–M4, generates the quadratic term corresponding to $(X+Y)^2$. The second loop, which includes devices M5–M8, similarly produces the quadratic term associated with $(X-Y)^2$. Together, these loops form the functional basis of the multiplication mechanism.

The current-domain relations that describe the behavior of each of the two translinear paths can be formulated as shown below:

$$I_{out} = \frac{I_X I_Y}{I_B} \tag{10}$$

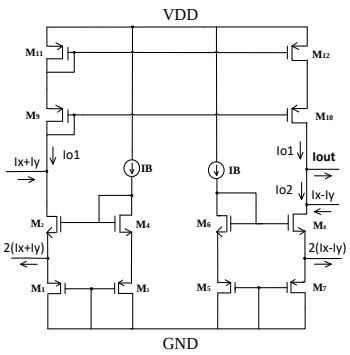


Fig. 3. Analog Multiplier Core

3. Simulation Results

The effectiveness of the proposed MIC was assessed through simulations carried out in the XFAB 0.18-µm CMOS process, operating with ±1.2 V supply. Stable operation was achieved by setting the bias currents IB1, IB2, IB3 to 30 µA, 40 µA, 50 µA, and IB4 to 80 µA, respectively. The circuit was then driven by a source with a peak amplitude of 1 mA, and its behavior was examined for bias conditions of 100 µA, 150 µA, and 200 µA. The resulting waveforms are presented in Fig. 4. In this configuration, the transconductances g_{m3} and g_{m2} were found to be 65 µA/V and 22 µA/V.

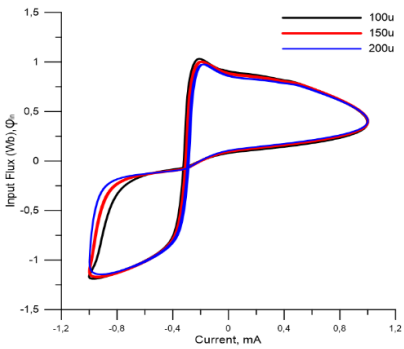
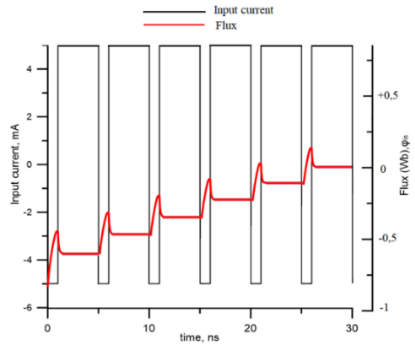


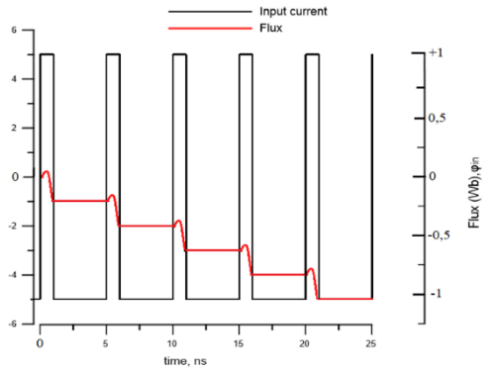
Fig. 4. Hysteresis response under various bias current levels

To investigate the memory-dependent behavior of the MIC, the circuit in Fig. 1 was stimulated with a train of current pulses. These pulses alternated from –5 mA to +5 mA and repeated every 5 ns, allowing the dynamic characteristics of the emulator to be observed.

Figure 5 presents the non-volatile operation of the proposed MIC for both a) increasing and b) decreasing modes, along with the corresponding changes in the meminductor flux. The plots show that the flux either rises or falls according to the direction of the applied current. Each new excitation pulse continues from the previously stored flux level, confirming that the emulator successfully reproduces the memory-dependent behavior expected from a meminductive element. In Fig. 6, when the circuit is excited with a 1 mA signal at 70, 80, and 90 MHz, the resulting current–flux trajectories are obtained.



(a)



(b)

Fig. 5. The proposed MIC exhibits non-volatile characteristics in both a) increasing and b) decreasing operating modes.

The design functions stably within the 60–90 MHz range and exhibits a total power consumption of 11.2 mW.

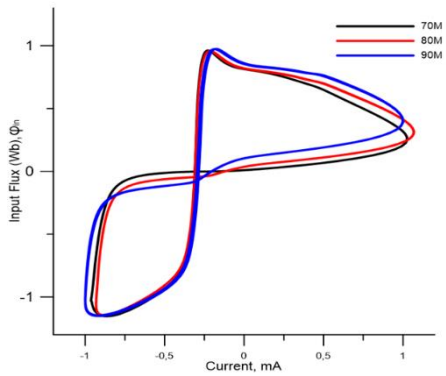


Fig. 6. Hysteresis curves exhibiting a pinched shape at three distinct operating frequencies

In addition, the circuit's resilience was examined by running simulations over a wide range of temperatures and process variations. As illustrated in Fig. 7, three distinct temperature levels were evaluated to observe the impact of significant thermal changes. The results indicate that the proposed design sustains stable and dependable performance, even when subjected to these challenging conditions

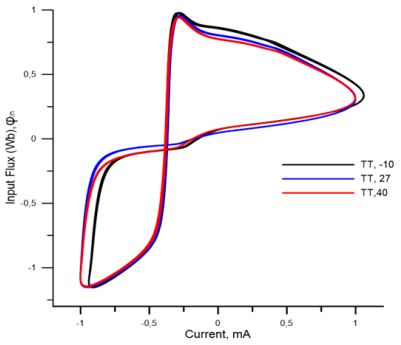


Fig. 7. At the nominal TT corner, pinched-type hysteresis characteristics are generated for three different temperature conditions.

4. Evaluation of Non-Ideal Effects in the MIC

When the frequency-dependent imperfections of the active components are taken into account, the MIC's non-ideal response can be described using the model illustrated in Fig. 8.
Analyzing this model directly leads to the following expression for the non-ideal input behavior [17]:

$$V_1 = [\alpha_1(s)\beta_1(s)\gamma_1(s)\frac{1}{\left(\frac{1}{r_{z1}}+sC_{P1}\right)}]I_{in} \qquad (11)$$

Here, r_{z1} denotes the inherent resistance linked to the z-terminal, while $\alpha_1(s)$ and $\beta_1(s)$ correspond to the CCCII's frequency-dependent current and voltage transfer gains, respectively. The term $\gamma 1(s)$ represents the unity-gain buffer's frequency-dependent voltage gain. Although each parameter can be expressed through a single-pole transfer form, the bandwidth of the current transfer function $\alpha_1(s)$ is considerably smaller compared to those of $\beta_1(s)$ and $\gamma_1(s)$. Consequently, in reducing Eq. (11), $\beta_1(s)$ and $\gamma_1(s)$ can be assumed to be constant. Under this consideration, $\alpha_1(s)$ is modeled using the following single-pole approximation:

$$\alpha_1(s) = \alpha_0 \frac{\omega_z}{s+\omega_z}. \qquad (12)$$

Here, α_0 represents the low-frequency current gain of the CCCII, which ideally is equal to unity. Moreover, when the CCCII's output resistance is chosen to be large enough so that the condition $(1/r_{z1} \ll |j\omega C_{P1}|)$ holds across the intended frequency band, Eq. (11) can be simplified to the following form:

$$V_1 \cong= \frac{\alpha_1(s)}{C_{P1}}\frac{I_{in}}{s} = \frac{\alpha_1(s)}{C_{P1}} q_{in} \qquad (13)$$

$$I_{z2} = g_{m2}V_1 = \frac{\alpha_1(s)g_{m2}}{C_{P1}} q_{in} \qquad (14)$$

The multiplier output:

$$I_{multiplier} = \frac{\alpha_1(s)g_{m2}}{C_{P1}} q_{in} \text{ x } I_{in} \qquad (15)$$

A standard analysis leads to the following expressions:

$$V_2 \cong \left[\alpha_3(s)g_{m3}\frac{1}{C_{P2}}\right]\varphi_{in} \qquad (16)$$

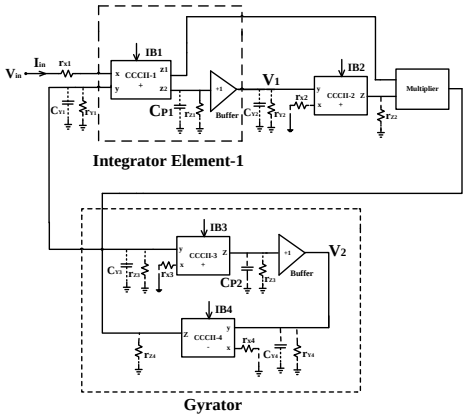


Fig. 8. Modeling the non-ideal characteristics of MIC

$$I_{multiplier} = \frac{V_2}{r_{x4}} = \left[\alpha_3(s)\frac{g_{m3}}{r_{x4}}\frac{1}{C_{P2}}\right]\varphi_{in} \qquad (17)$$

When expression (18) is inserted into (15), the resulting relation takes the following form:

$$\left[\alpha_3(s)\frac{g_{m3}}{r_{x4}}\frac{1}{C_{P2}}\right]\varphi_{in} = \frac{\alpha_1(s)g_{m2}}{C_{P1}} q_{in} \text{ x } I_{in} \qquad (18)$$

$$L_M = \frac{\varphi_{in}}{I_{in}} = \frac{\alpha_1(s)}{\alpha_3(s)}\frac{g_{m2}}{g_{m3}}\frac{C_{P2}}{C_{P1}} q_{in}\, r_{x4} \qquad (19)$$

In this representation, αk(s) (k=1,2) corresponds to the current-transfer behavior of the CCCIIs as a function of frequency. The components of the expression are determined by evaluating the transfer function at s=*jω*

5. Comparison with Previously Reported Meminductor Implementations

A selection of the most recent and closely related designs is summarized in Table 2. Although the number of active components used in the proposed circuit is similar to that of other implementations, the absence of any passive elements is a key advantage, as it can lead to a significantly smaller silicon footprint.

6. Conclusions

It is proposed an active-only meminductor consists of a voltage follower, a CCCII, and a multiplier, removing the necessity for any passive elements. Since the design relies exclusively on active components, it offers a significantly reduced silicon footprint, which in turn supports further shrinkage in integrated circuit area—an important benefit for practical implementation. The findings also show that the circuit maintains efficient high-frequency performance, primarily due to the utilization of intrinsic MOS gate capacitances. It is validated the behavior of the proposed meminductor structure and clearly reveal its memory-dependent characteristics by obtaining simulation results. Moreover, the non-ideal aspects of the system are examined thoroughly. The functionality of the proposed architecture is confirmed through Spectre simulations carried out using the XFAB 0.18-µm CMOS process.

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Table 2. Performance comparison of the proposed emulator with earlier meminductor circuits

Ref.	Count of active components.	Technology	Op. Freq.	Count of passive components	Type of component	Elec. Tunability
[20]	2 OTAs, 1 Multiplier	Experimental and TSMC 0.18µm	10 kHz	2R, 2C	Grounded	Yes
[19]	2 VDTA	Cadence gpdk 0.18µm/ Experimental	1 MHz	1R, 2C	Both	Yes
[12]	1 DOCCII, 1 CCII, 1 AM	LTSPICE/ Experimental	700 kHz	2R, 2C, 1L	Grounded	No
[18]	1VDTA 1 OTA	Cadence gpdk 0.18µm	3 MHz	2C	Grounded	Yes
This study	**2 CFOAs, 1 CCCII, 1 multiplier**	**XFAB 0.18µm**	**90 MHz**	**No passive elements**	**Grounded**	**Yes**