Fully Active Meminductor Emulator Circuit

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Abstract

This paper introduces an active-only meminductor circuit, uniquely designed to emulate the meminductor without the need for external capacitors, relying solely on the internal capacitor of transistors. This innovative approach minimizes the circuit's footprint on the integrated circuit (IC) environment. Simulation results conducted in the Cadence design environment, employing the 0.18 µm CMOS process, validate the theoretical study's effectiveness.

Keywords: Meminductor emulator circuit, Memory behaviour, Active-only design

1. Introduction

A memristor, a basic passive circuit component that combines flux and charge, was first conceptualized by Leon Chua [1,2]. Memory circuit components have been extended to capacitive and inductive systems as a result of the memristor concept's success [3].

Like memristors, memcapacitors and meminductors have a memory property, shown by a closed, pinched hysteresis loop between their two state variables. They also have the added benefit of storing energy in capacitive and inductive forms, respectively [4]. These features make them promising for mimicking biological computation, and they are expected to play an important role in the development of neuromorphic computing. Because they can store and process information at the same time, computers built with these mem-elements could offer brain-like capabilities with low power consumption [5–7]. However, the absence of solid-state versions of memcapacitors and meminductors limits their use in real applications. For this reason, recent research has focused on building emulator circuits that reproduce the equations and behavior of these devices.

A wide range of meminductor emulator designs reported in the literature reproduce the characteristic behaviour of these elements by employing various combinations of analog active building blocks together with passive components. For example, a mutator-based implementation utilized two current conveyors, one buffer, one multiplier, two current sources, and passive elements [8]. A memristor-less current-controlled version was realized with three current conveyors, one adder, one multiplier, and five passive components, while its voltage-controlled counterpart incorporated three current conveyors, one summer, one divider, and the same number of passive elements [9]. Another reported design comprised twelve MOSFETs, one multiplier, three operational amplifiers, and passive elements [10]. An alternative topology integrated one buffer, one multiplier, two operational amplifiers, four current conveyors, and eight passive elements [11]. Similarly, other mutator-based emulators were constructed using one multiplier, two operational amplifiers, two current conveyors, and eight passive elements [12]. Additional examples include a compact adder–subtractor configuration with three passive elements [13] and a circuit with twelve passive elements, one multiplier, and five operational amplifiers [14]. Gyrator-based approaches have employed six passive components and two operational amplifiers [15]. Floating mutator-based designs featured one operational amplifier, four current conveyors, one varicap diode, and six passive elements [16], whereas another design used three current conveyors, five passive components, and one analog multiplier [17]. Hybrid configurations have been implemented with ten passive components, one operational amplifier, three current conveyors, one multiplier, and one operational transconductance amplifier [18]. A simpler version was also demonstrated using one capacitor, two operational amplifiers, one memristor, and three resistors [19].

Nevertheless, these designs generally include external passive components like capacitors, inductors, and resistors, following conventional circuit design methods. The reliance on passive elements presents significant challenges, including increased chip area and elevated power consumption, which are major concerns in applications demanding minimal footprint.

The primary objective of this work is to design a meminductor emulator circuit (MIC) that eliminates the reliance on passive components, thereby overcoming their associated limitations. The proposed MIC is realized entirely with active elements, and its performance is comprehensively evaluated in comparison with previously published circuits. Extensive simulations were performed using the XFAB 0.18 µm CMOS process, and an equivalent model of the circuit was analysed to investigate the influence of key non-ideal characteristics.

The organization of the paper is as follows: Section 2 introduces the overall topology and theoretical background of the proposed MIC. Section 3 presents the simulation results, while Section 4 discusses the impact of non-idealities on circuit performance. A comparative study with existing designs is given in Section 5. Finally, Section 6 concludes the paper with a summary of the findings.

2. Circuit Realization of Proposed MIC

The definition of the meminductor element can be done as follows:

$$\varphi_L(t) = L_M[\int_{t_0}^{t} i(\tau)d\tau]i(t) = L_M(q)i(t). \qquad (1)$$

It is known as charge-controlled meminductor. Here, input flux (φ) is the integral of the input voltage.

The structure of MIC is illustrated in Fig. 1. The emulator circuit is realized solely by active elements, without the need for any external passive components, utilizing the intrinsic capacitances of the active devices.

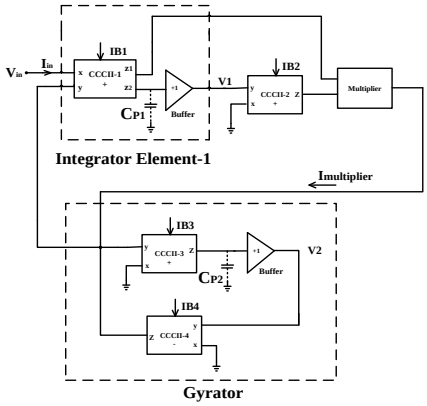

Fig. 1. Proposed meminductor emulator circuit

Accordingly, the characteristic equations of the designed circuit can be derived as follows:

$$V_1 = \frac{1}{C_{P_1}} \int I_{in}(t)dt = \frac{q_{in}}{C_{P_1}} \tag{2}$$

$$I_{z2} = g_{m2} V_1 = \frac{g_{m2}}{C_{P_1}}\, q_{in} \tag{3}$$

The multiplier output:

$$I_{multiplier} = \frac{g_{m2}}{C_{P_1}}\, q_{in} \text{ x } I_{in} \tag{4}$$

After routine analysis of the gyrator, it is obtained the following equations:

$$V_2 = \frac{1}{C_{P2} r_{x3}} \int V_{in}(t)dt = \frac{g_{m3}}{C_{P2}}\, \varphi_{in} \tag{5}$$

$$I_{multiplier} = \frac{V_2}{r_{x4}} = \frac{g_{m3}}{r_{x4}\, C_{P2}}\, \varphi_{in} \tag{6}$$

By substituting (6) in (4), the equation is obtained as follows:

$$\frac{g_{m3}}{r_{x4}\, C_{P2}}\, \varphi_{in} = \frac{g_{m2}}{C_{P_1}}\, q_{in}\, x\, I_{in} \tag{7}$$

$$L_M = \frac{\varphi_{in}}{I_{in}} = \frac{g_{m2}}{g_{m3}} \frac{C_{P2}}{C_{P_1}}\, q_{in}\, r_{x4} \tag{8}$$

Fig.2a depicts the CCCII active element, realized through a conventional translinear architecture. The voltage buffer is presented in Fig.2b.

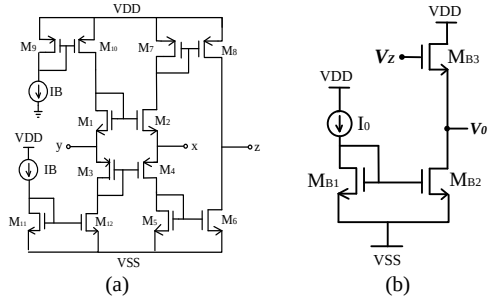

Fig. 2. (a) CMOS-based design of the CCCII [20], (b) Voltage follower circuit

In this study, a novel meminductor circuit is proposed that eliminates the need for passive components, resulting in significant savings in chip area. This is achieved by leveraging the gate capacitances of MOSFETs operating in the saturation region. Additionally, the use of MOS transistors with enlarged gate areas within the circuit design helps to mitigate the effects of nonlinear junction capacitances. Compared to traditional metal-plate capacitors, MOS transistors offer a higher capacitance density, contributing to a minimized chip area [21]. During the design process of the circuit shown in Fig. 1, particular attention was given to optimizing transistor sizing: The transistors within the CCCII were kept as small as possible to enhance high-frequency performance, while the MOS transistors at the input stage of the voltage follower were deliberately enlarged to increase the parasitic capacitance at its input terminal. The transistor sizes utilized in the CCCII and voltage buffer are shown in Table 1.

Table 1. Transistor sizes used in the CCCII element

MOS transistor	CCCII
M_1-M_2	4µm/0.8µm
M_3-M_4	10µm/0.8µm
M_5	2µm/0.8µm
M_6	5µm/0.8µm
M_7	1.5µm/0.8µm
M_8	4µm/0.8µm
M_9-M_{10}	4µm/0.8µm
M_{11}-M_{12}	2µm/0.8µm
M_{B3} (voltage buffer)	35 µm/0.8 µm
M_{B1}-M_{B2} (voltage buffer)	2µm/0.8µm

2.1. Multiplier Subcircuit

This sub-circuit, responsible for the multiplication operation, can be implemented using the following equation [22]:

$$(X+Y)^2 - (X-Y)^2 = 4XY \tag{9}$$

As illustrated in Fig. 3, the circuit operates based on two translinear loops, which enable squaring operations. The first loop, consisting of transistors M1–M4, realizes the squaring function $(X+Y)^2$, while the second loop, formed by transistors M5–M8, performs the squaring function $(X-Y)^2$.

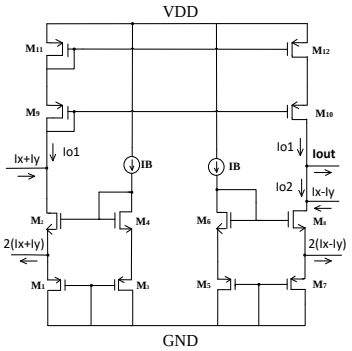

Fig. 3. Multiplication circuit block

The mathematical expressions corresponding to the operations of these two loops, in terms of current values, are given as follows:

$$I_{out} = \frac{I_X I_Y}{I_B} \tag{10}$$

3. Simulation Results

In order to validate the effectiveness of the proposed design, MIC was implemented using the 0.18 µm XFAB technology with a supply voltage of ±1.2 V. For its proper functionality, the bias currents IB1, IB2, IB3 and IB4 were set to 20 µA, 30 µA, 40 µA, and 100 µA, respectively. When the proposed MIC was driven by a sinusoidal input current with a peak amplitude of 1 mA under biasing currents of 100 µA, 150 µA, and 200 µA, the resulting characteristics were obtained as shown in Fig. 4. The values of g_{m2} and g_{m3} are 22 µA/V and 65 µA/V, respectively.

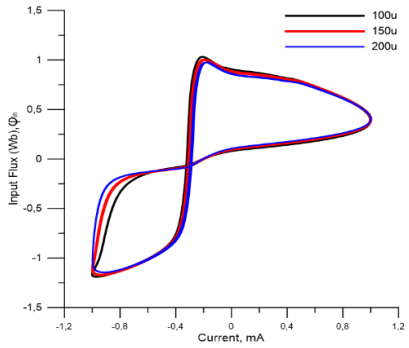

Fig. 4. Hysteresis behavior corresponding to different biasing conditions.

To examine the memory characteristics of MIC, a sequence of current pulses with amplitudes varying between –5 mA and +5 mA and a period of 5 ns was applied to the input of the circuit illustrated in Fig. 1.

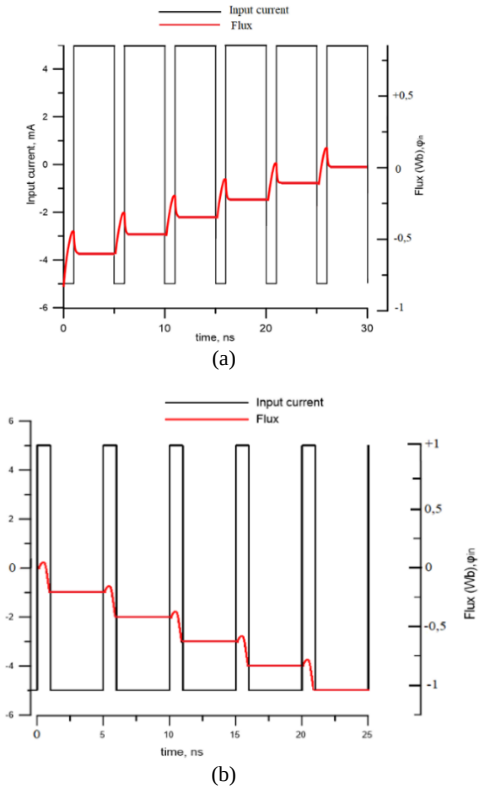

Fig. 5. Non-volatile behavior of the proposed MIC under a) incremental and b) decremental configurations.

The corresponding variations in the meminductor's flux are depicted in Fig.5.

It can be clearly seen that the flux increases or decreases depending on the current direction. Furthermore, each subsequent pulse resumes the flux from its previous state, verifying that the emulator circuit effectively demonstrates the memory property of a meminductor. As shown in Fig. 6, when the meminductor emulator is driven by a 1 mA input current at 70 MHz, 80 MHz, and 90 MHz, the corresponding current–flux characteristics are obtained. The proposed circuit operates within the frequency range of 60–90 MHz. The power consumption of the proposed circuit is 11.2mW.

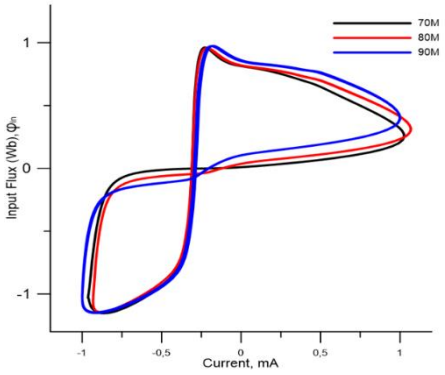

Fig. 6. Pinched hysteresis loops for three different frequencies.

Furthermore, to assess the robustness of the circuit under diverse operating scenarios, simulations were performed across multiple temperatures and process corners. As shown in Fig. 7, the design was analysed at three separate temperature points to investigate the influence of considerable thermal variations. The findings demonstrate that the proposed circuit continues to operate reliably, even under such demanding conditions.

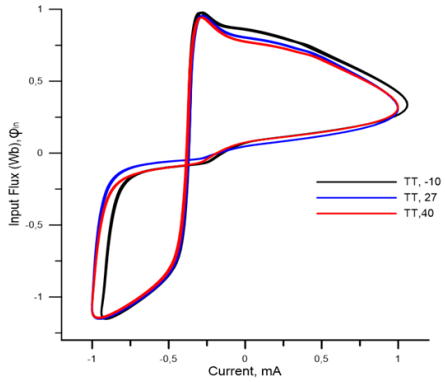

Fig. 7. Hysteresis loops with pinched shape obtained at the nominal TT process corner for three temperature levels.

4. Non-Ideal Analysis of MIC

Taking into account the frequency-dependent imperfections of the active components, the non-ideal behavior of MIC is modeled, as illustrated in Fig.8.

A straightforward analysis of this model produces the following non-ideal input characteristic [23]:

$$V_1 = [\alpha_1(s)\beta_1(s)\gamma_1(s)\frac{1}{\left(\frac{1}{r_{z1}}+sC_{P1}\right)}]I_{in} \quad (11)$$

Here, r_{z1} denotes the intrinsic resistance at the z-terminal, while $\alpha_1(s)$ and $\beta_1(s)$ represent the frequency-dependent current and voltage gains of the CCCII, respectively. Moreover, $\gamma_1(s)$ corresponds to the frequency-dependent voltage gain of the unity-gain voltage buffer. Although each of these non-ideal parameters can be represented by a single-pole transfer function, the bandwidth of the non-ideal current transfer function is considerably smaller compared to those of $\beta_1(s)$ and $\gamma_1(s)$. Thus, Eq. (11) can be simplified by assuming $\beta_1(s)$ and $\gamma_1(s)$ as constants. Accordingly, $\alpha_1(s)$ can be expressed using a single-pole model as follows:

$$\alpha_1(s) = \alpha_0 \frac{\omega_z}{s+\omega_z}. \quad (12)$$

where α_0 denotes the low-frequency gain of the CCCII, whose ideal value equals 1.

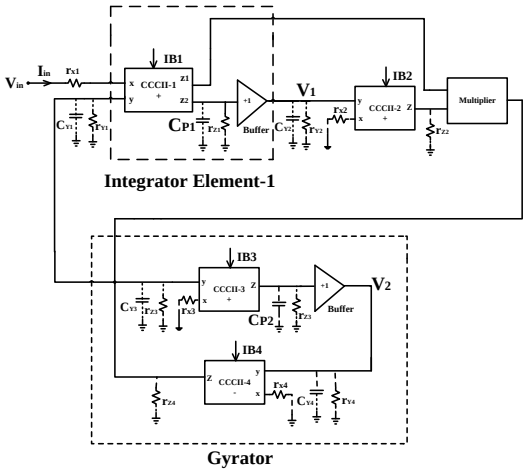

Fig. 8. Non-ideal representation of the proposed meminductor emulator circuit

Furthermore, if the circuit is designed such that the output resistance of the CCCII is sufficiently high to satisfy the condition $(1/r_{z1} \ll |j\omega C_{P1}|)$ within the operating frequency range, Eq. (11) can be approximated as:

$$V_1 \cong= \frac{\alpha_1(s)}{C_{P1}}\frac{I_{in}}{s} = \frac{\alpha_1(s)}{C_{P1}}\mathrm{q}_{in} \quad (13)$$

$$I_{z2} = \mathrm{g}_{m2}V_1 = \frac{\alpha_1(s)g_{m2}}{C_{P1}}\mathrm{q}_{in} \quad (14)$$

The multiplier output:

$$I_{multiplier} = \frac{\alpha_1(s)g_{m2}}{C_{P1}}\mathrm{q}_{in}\ \mathrm{x}\ I_{in} \quad (15)$$

After routine analysis of the gyrator, it is obtained the following equations:

$$V_2 = \alpha_3(s)\beta_3(s)\gamma_3(s)\frac{V_{in}}{(sC_{P2}+\frac{1}{r_{z3}})r_{x3}} = \alpha_3(s)\beta_3(s)\gamma_3(s)\frac{g_{m3}}{(sC_{P2}+\frac{1}{r_{z3}})}V_{in} \quad (16)$$

$$V_2 \cong \left[\alpha_3(s)g_{m3}\frac{1}{C_{P2}}\right]\varphi_{in} \quad (17)$$

$$I_{multiplier} = \frac{V_2}{r_{x4}} = \left[\alpha_3(s)\frac{g_{m3}}{r_{x4}}\frac{1}{C_{P2}}\right]\varphi_{in} \quad (18)$$

By substituting (18) into (15), the equation is obtained as follows:

$$\left[\alpha_3(s)\frac{g_{m3}}{r_{x4}}\frac{1}{C_{P2}}\right]\varphi_{in} = \frac{\alpha_1(s)g_{m2}}{C_{P1}}\mathrm{q}_{in}\ \mathrm{x}\ I_{in} \quad (19)$$

$$L_M = \frac{\varphi_{in}}{I_{in}} = \frac{\alpha_1(s)}{\alpha_3(s)}\frac{g_{m2}}{g_{m3}}\frac{C_{P2}}{C_{P1}}\mathrm{q}_{in}\ r_{x4} \quad (20)$$

where αk(s) (k=1,2) represent the frequency-dependent current gains of the CCCIIs. The terms in the above expression are obtained by substituting s=jω.

5. Comparison with Existing Circuits in the Literature

To assess the performance of the proposed MIC, it has been compared with related works reported in the literature. The most relevant and recent examples are summarized in Table 2. While the proposed emulator employs a comparable number of active devices to other designs, it requires no passive components, which is expected to further reduce the overall chip area.

6. Conclusions

This study introduces a novel active-only Meminductor Emulator Circuit (MIC) employing elements such as CCCII, voltage buffer, and multiplier. Notably, it eliminates passive elements. This design choice results in a significantly reduced footprint on the integrated circuit (IC), which is expected to further decrease the chip area, providing a crucial advantage for practical circuit implementation. Comprehensive simulation results validate the effectiveness of the proposed meminductor emulator and demonstrate the memory behavior of the proposed circuit. The results highlight the circuit's capability to operate at high frequencies, attributed to the exclusive use of intrinsic gate capacitors in its design. Furthermore, the study delves into the investigation of non-ideal effects of the circuit. The proper functioning of the proposed circuit is demonstrated through Spectre simulation results conducted in the Cadence design environment, utilizing the XFAB 0.18µm process.

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Table 2. Comparison of proposed meminductor emulators with other presented meminductor emulators

Ref.	# of active comp.	Op. Freq.	# of passive comp.	Element type	Elec. Tunability	Transistor Parameter
[17]	3 CCIIs, 1 Multiplier	5 kHz	2C, 3R	Grounded	No	Experimental
[18]	2 CCIIs, 1 CFOA, 1 Opamp, 1 Multiplier	5 kHz	2C, 7R	Both	Yes	Experimental
[19]	2 Opamp, 1 Multiplier	2 MHz	1C, 3R, 1 M_R	Grounded	NA	Experimental
[24]	2 OTAs, 1 Multiplier	10 kHz	2R, 2C	Grounded	Yes	Experimental and TSMC 0.18µm
[25]	2 VDTA	1 MHz	1R, 2C	Both	Yes	Cadence gpdk 0.18µm/ Experimental
[26]	2-DDCCs, 1-Multiplier, 1 Transistor	1.5 kHz	2R, 1C	Grounded	Yes	TSMC 0.35 µm CMOS
[27]	1 MVDCC, 1 OTA	300 kHz	1R, 2C	Floating	Yes	PSPICE/ Experimental
Prop. work	**2 CFOAs, 1 CCCII, 1 multiplier**	**90 MHz**	**No passive elements**	**Grounded**	**Yes**	**XFAB 0.18µm**

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